IN610 IN610L IN612L Datasheet

Specifications and information are subject to change without notice.

IN610 IN610L IN612L

Bluetooth Low Energy 5 & Software-Defined Radio Wireless SoC

Key Features

- **Multi-mode collaborative protocol stack**
  - Bluetooth® low energy (BLE) 5
    - Bluetooth® low energy 5 spec fully compliant
    - High data rate up to 2 Mbps
    - Long range mode (125 kbps/500 kbps)
    - Advertising extension support
  - SDR (Software defined radio, user defined)
    - Flexible Rx/Tx enable control
    - Event triggering mode for low power design
    - Bidirectional wireless communication
    - Concurrent with BLE 5 operation

- **CPU & memory**
  - ARM® Cortex®-M4F up to 64MHz with 16KB i-cache
  - 256KB ROM (bootloader & SW stack)
  - Up to 96KB SRAM for data/instruction
  - 4Kb eFuse memory (manufacturer ID, security key storage)
  - 512KB Flash memory (stacked, XIP mode support)
  - Over-the-air (OTA) update support
  - SWD/JTAG debug interface

- **Radio**
  - 2.4GHz transceiver, Bluetooth® 5 compliant
  - Rx sensitivity -104.5 dBm @ 125Kbps
  - Rx sensitivity -97.5 dBm @ 1Mbps
  - Rx sensitivity -94.5 dBm @ 2Mbps
  - Tx output 0dBm, 4.9mA, up to +3 dBm
  - Rx 5mA
  - Link budget of 107.5 dB @ 125Kbps
  - MedRadio Band Support (2360MHz~2400MHz)

- **Peripherals**
  - Up to 30 GPIOs
  - 2 I2C, master/slave up to 1000kHz clock
  - 1 SPI master w/ up to 4 SPI slaves supported, up to 16MHz clock
  - 1 SPI slave, up to 8MHz
  - 2 UART up to 2MHz
  - 5 dedicated PWMs, up to 13 PWM through I/O configuration
  - 1 I2S master and 1 I2S slave, bidirectional stereo support
  - 2 PDM mono or 1 stereo with clock range from 160kHz – 5.12MHz
  - ISO7816
  - Keyboard scanner – up to 14x14 matrix
  - Quadrature decoder
  - 11-bit ADC, up to up to 64 KSPS, up to 12 channels
  - 8 counters/timers

- **External Clock sources**
  - 32MHz crystal,31/32.768 kHz RTC

- **DMA Controller**
  - Up to 2 concurrent DMA streams with 2 channels each

- **Voice/Audio engine**
  - Build-in stereo/mono ADPCM codec with 4:1 compression
  - Support both ADPCM and raw PCM as output with sampling frequency up to 64kHz
  - PDM or I2S input
  - Sigma-delta audio DAC output

- **Security**
  - Hardware ECC, AES, SHA-1, SHA-2 engines
  - Secure boot, software copyright protection
  - True random number generator (TRNG)

- **Power mode**
  - Deep sleep mode 500nA with 32kHz RC ON
  - Shutdown mode < 20nA

- **PMU**
  - Integrated DCDC buck convertor
  - 1.65V - 3.6V input

- **Packaging**
  - QFN48 6x6mm

- **Operating temperature**
  - -40 ~ +85 °C

- **Typical applications**
  - IoT applications
  - Bluetooth Gateway
  - Smart home automation, smart lighting
  - Industrial IoT
  - Wearables, toys
  - Asset tracking management
  - Smart retail applications
  - Connected appliances, locks.

About Documentation

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Product type number	IN610, IN610L and IN612L	
Control number	IN6IDOC-DS-IN612L-EN-V2_00	For external use
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Product status	Document content	Data status
In development	Objective Specification/MRD	Target Specification. Revised and supplementary data will be published later
Engineering sample	Specification with measured data on E/S	Data based on early E/S sample testing
Customer sample	Specification with measured data on the early production samples	Data based on early production samples. Revised and supplementary data may be published later.
Mass production		The document contains the final product specification

This document applies to the following products:

Product type	Part number	Product status
IN610	IN610-Q1-R-G4C0I	Mass production
IN610L	IN610L-Q1-R-G4C0I	Mass Production
IN612L	IN612L-Q1-R-G4C0I	Mass Production

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1 Product Overview

IN610, **IN610L** and **IN612L (IN6XX)** are SoC devices that belong to the SwiftRadio™ SoC IN6XX product family. The product family features a multi-mode collaborative protocol stack that runs on an MCU with an integrated 2.4GHz frequency band RF radio. The product integrates user-friendly software-defined radio (SDR) and Bluetooth® low energy (BLE) 5. BLE is fully compliant with the standard specification and includes 2Mbps high data rate mode, 125Kbps/500Kbps coded PHY rate support as well as extended advertising capabilities. The user-defined SDR stack and its built-in BLE stack can be operated concurrently so that many complex networking applications can be designed and optimized.

The device integrates a powerful 32-bit ARM® Cortex®-M4F CPU with an integrated floating-point processing unit. It has a built-in 256KB ROM and a data/instruction SRAM of 96KB, and a 512 KB flash memory. The flash memory is a stacked flash memory. Inside the IN6XX package, there are two dies: the main MCU die and the flash die. The flash is stacked on top of the MCU die (as shown in Figure 1). The MCU die contains all function blocks except the flash memory. The MCU accesses the flash through a dedicated QSPI interface.

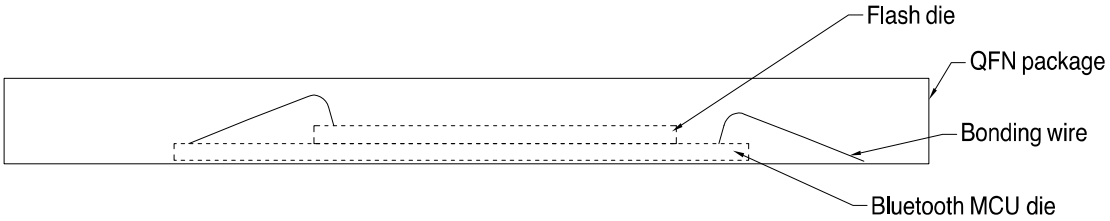


Figure 1: The flash die and the main Bluetooth MCU die inside the QFN package

The device has excellent RF performance designed with ultra-low power consumption in mind, so it is well suited for power constrained applications such as battery-powered products (ex. retail beacons and wearables). Along with the powerful ARM Cortex-M4F CPU and rich memory resources integrated into the device, users can develop many applications without adding additional CPUs.

The device integrates various hardware security engines/accelerators which support AES-128, AES-256, SHA-1, SHA-2, and Elliptic-curve cryptography (ECC). It integrates a true random number generator (TRNG) which facilitates security applications.

In addition to the sophisticated design of the radio and communication modems, the device integrates an audio engine and a variety of peripherals such as I2C, SPI, UART, PDM, and I2S for user applications.

Figure 2 shows the system block diagram of the SwiftRadio™ SoC IN6XX product family. The shared memory (40KB) is a dedicated memory shared and used by the BLE baseband and the audio engines.

In the SwiftRadio™ SoC product family, there are three product types: IN610, IN610L, and IN612L. The three products support the same feature set except those listed in Table 1.

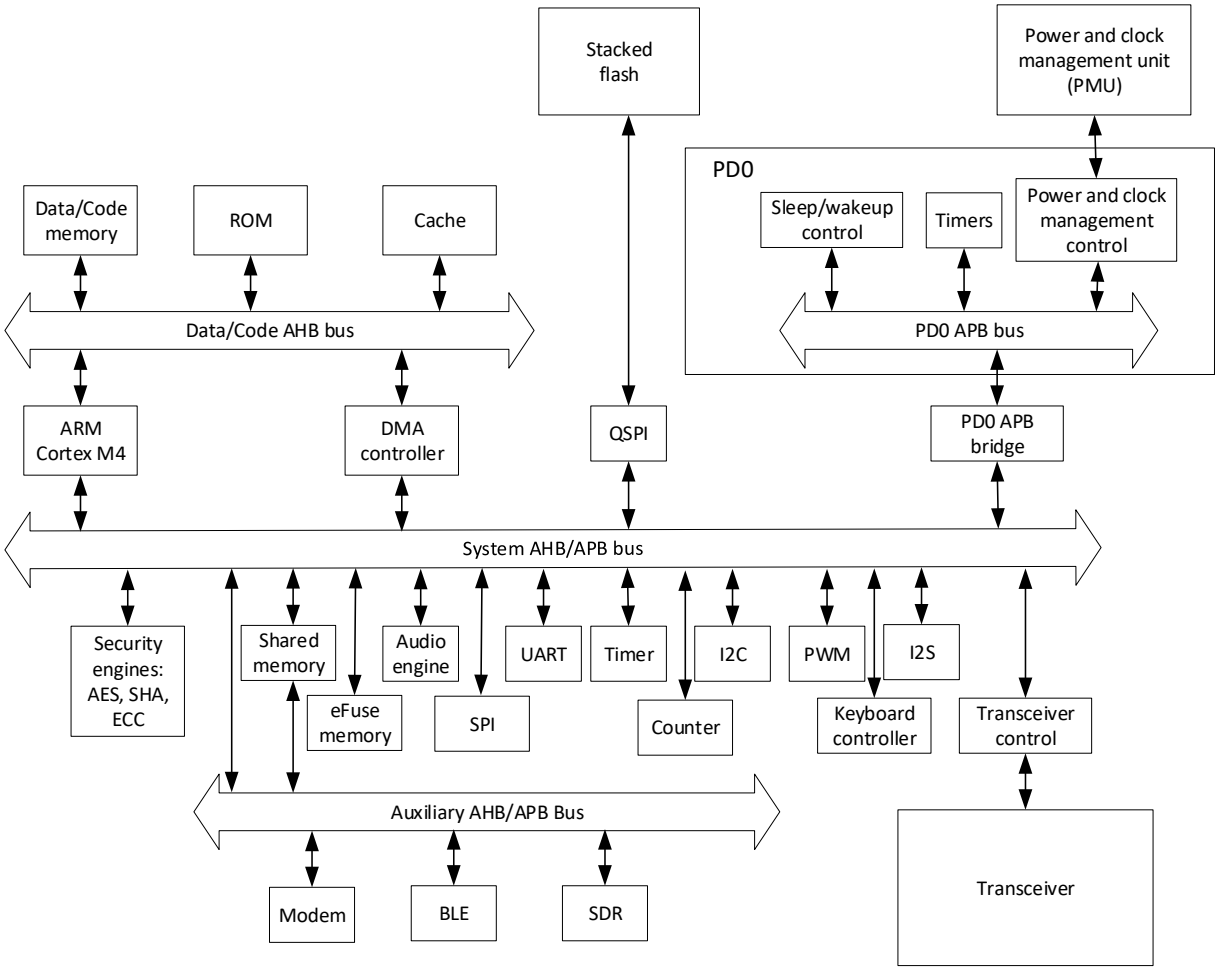


Figure 2: Device system block diagram

Table 1: Product types and feature differences

Feature	Product		
	IN612L	IN610L	IN610
Software-defined radio (SDR)	Supported	Not supported	Not supported
Coded BLE PHY rate (125 Kbps, 500Kbps)	Supported	Supported	Not supported

For the product type IN610 devices, there are multiple part numbers available, with different boot ROM features. For more information on available features of different device order part numbers, please refer to Ordering Information in section 5.

2 Pin Map Information

2.1 QFN 48

IN610, IN610L and IN612L (collectively, they are called IN6XX devices) are offered in a 48-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. In Figure 3, the QFN package pin assignment is shown. Table 2 shows the pin name, pin type and pin description.

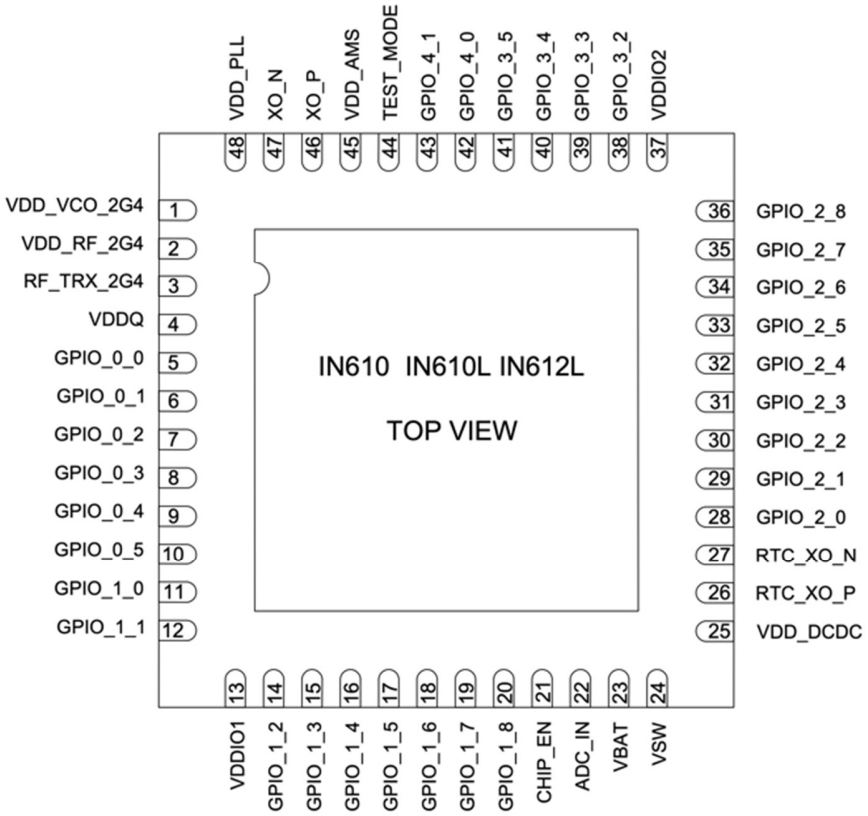


Figure 3: IN610/IN610L/IN612L pin assignment of QFN48

Table 2: IN610/IN610L/IN612L QFN48 pin description

Pin #	Pin name	Pin type	Description
1	VDD_VCO_2G4	Power	1.2V RF VCO power supply
2	VDD_RF_2G4	Power	1.2V RF power supply
3	RF_TRX_2G4	RF I/O	RF port
4	VDDQ	Power	The 3.3V eFuse programming voltage supply
5	GPIO_0_0	Digital I/O	General purpose digital I/O pin
6	GPIO_0_1	Digital I/O	General purpose digital I/O pin
7	GPIO_0_2	Digital I/O	General purpose digital I/O pin

Pin #	Pin name	Pin type	Description
8	GPIO_0_3	Digital I/O	General purpose digital I/O pin
9	GPIO_0_4	Digital I/O	General purpose digital I/O pin
10	GPIO_0_5	Digital I/O	General purpose digital I/O pin
11	GPIO_1_0	Digital I/O	General purpose digital I/O pin
12	GPIO_1_1	Digital I/O	General purpose digital I/O pin
13	VDDIO1*	I/O power	I/O voltage supply for digital IO power domain 1
14	GPIO_1_2	Digital I/O	General purpose digital I/O pin
15	GPIO_1_3	Digital I/O	General purpose digital I/O pin
16	GPIO_1_4	Digital I/O	General purpose digital I/O pin
17	GPIO_1_5	Digital I/O	General purpose digital I/O pin
18	GPIO_1_6	Digital I/O	General purpose digital I/O pin
19	GPIO_1_7	Digital I/O	General purpose digital I/O pin
20	GPIO_1_8	Digital I/O	General purpose digital I/O pin
21	CHIP_EN	Analog input	Chip enable
22	ADC_IN	Analog input	Sensor ADC input pin. The maximum input voltage is 2.0V on this pin.
23	VBAT	Power	Chip power supply
24	VSW	Power	DCDC converter switching node
25	VDD_DCDC	Power	DCDC converter feedback node
26	RTC_XO_P	Analog I/O	32.768 kHz crystal oscillator pin (positive terminal)
27	RTC_XO_N	Analog I/O	32.768 kHz crystal oscillator pin (negative terminal)
28	GPIO_2_0	Mixed signal I/O**	General purpose digital I/O and analog input pin
29	GPIO_2_1	Mixed signal I/O**	General purpose digital I/O and analog input pin
30	GPIO_2_2	Mixed signal I/O**	General purpose digital I/O and analog input pin
31	GPIO_2_3	Mixed signal I/O**	General purpose digital I/O and analog input pin
32	GPIO_2_4	Mixed signal I/O**	General purpose digital I/O and analog input pin
33	GPIO_2_5	Mixed signal I/O**	General purpose digital I/O and analog input pin
34	GPIO_2_6	Mixed signal I/O**	General purpose digital I/O and analog input pin
35	GPIO_2_7	Mixed signal I/O**	General purpose digital I/O and analog input pin
36	GPIO_2_8	Mixed signal I/O**	General purpose digital I/O and analog input pin
37	VDDIO2*	I/O power	I/O voltage supply for digital IO power domain 2
38	GPIO_3_2	Digital I/O	General purpose digital I/O pin
39	GPIO_3_3	Digital I/O	General purpose digital I/O pin
40	GPIO_3_4	Digital I/O	General purpose digital I/O pin

Pin #	Pin name	Pin type	Description
41	GPIO_3_5	Digital I/O	General purpose digital I/O pin
42	GPIO_4_0	Digital I/O	General purpose digital I/O pin
43	GPIO_4_1	Digital I/O	General purpose digital I/O pin
44	TEST_MODE***	Digital input	Test mode selection, GND for normal operation
45	VDD_AMS	Power	1.2V AMS (analog and mixed signal circuit) supply
46	XO_P	Analog I/O	32 MHz crystal oscillator pin (positive terminal)
47	XO_N	Analog I/O	32 MHz crystal oscillator pin (negative terminal)
48	VDD_PLL	Power	1.2V RF PLL power supply

*: GPIO_0_X and GPIO_1_X pins are in the IO power domain 1 (VDDIO1), GPIO_2_X, GPIO_3_X, GPIO_4_X and TEST_MODE pins are in the VDDIO2 domain.

**: The mixed signal I/O (GPIO_2_X) pins can be configured as an analog input pin to the sensor ADC by software. When a mixed signal GPIO pin is configured as an analog input pin, the input voltage on that pin should not be beyond 2.0V. These pins are configured as digital I/O pins by default.

***: If the TEST_MODE pin is connected to GND, the device will be in normal operation mode. If it is connected to "high" (>=0.7 *VDDIO2), the device will be in scan test mode. This pin does not have internal pull-up or pull-down resistor.

TEST_MODE pin enables the device to enter the scan chain test mode used during chip manufacturing. When the device enters scan chain test mode, the chip's internal circuitry is configured to perform only scan chain testing. In scan chain testing, the chip's functional elements are connected in a chain-like structure, allowing for more efficient testing of the chip's internal logic and normal functionality of the device such as CPU, Bluetooth, and etc., will no longer be available.

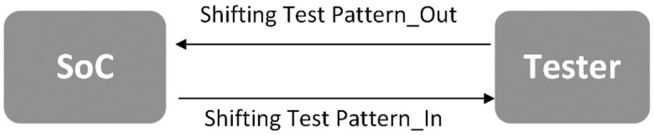


Figure 4: Test mode data flow

Table 3 shows the pin mux configuration that user can use to configure the digital I/O functionality based on application needs.

Table 3: GPIO pin mux

Pin #	Pin name	MUX Option	I/O	Description
5	GPIO_0_0	0	I/O	General purpose I/O
		1	O	UART 0 RTS
		2	I/O	Keyboard pin 0
		3		N/A

Pin #	Pin name	MUX Option	I/O	Description
		4	I/O	I2C 0 SCL
		5		N/A
		6	O	PWM 0
6	GPIO_0_1	0	I/O	General purpose I/O
		1	I	UART 0 CTS
		2	I/O	Keyboard pin 1
		3	I	SPI master MISO
		4	I/O	I2C 0 SDA
		5		N/A
		6	O	PWM 1
7	GPIO_0_2	0	I/O	General purpose I/O
		1	O	UART 0 TXD
		2	I/O	Keyboard pin 2
		3, 4, 5		N/A
		6	O	PWM 2
8	GPIO_0_3	0	I/O	General purpose I/O
		1	I	WLAN TX signal (for WIFI/BLE coexistence)
		2	I/O	Keyboard pin 3
		3	O	SPI master MOSI
		4	I/O	I2C 1 SCL
		5	O	Audio sigma/delta output left channel
		6	O	BLE TX enable indicator
9	GPIO_0_4	0	I/O	General purpose I/O
		1	I	WLAN Rx signal (for WIFI/BLE coexistence)
		2	I/O	Keyboard pin 4
		3	O	SPI master clock (CLK)
		4	I/O	I2C 1 SDA
		5	O	Audio sigma/delta output right channel
		6	O	BLE TX enable indicator
10	GPIO_0_5	0	I/O	General purpose I/O
		1		N/A
		2	I/O	Keyboard pin 5
		3, 4, 5, 6		N/A
11	GPIO_1_0	0	I/O	General purpose I/O
		1	I	UART 0 RXD
		2	I/O	Keyboard pin 6
		3, 4, 5		N/A
		6	O	ETM TRACECLK
12	GPIO_1_1	0	I/O	General purpose I/O
		1	I/O	SWDIO/JTAG TMS
		2, 3, 4, 5, 6		N/A
14	GPIO_1_2	0	I/O	General purpose I/O
		1	I	SWDCLK/JTAG TCK
		2, 3, 4, 5, 6		N/A
15	GPIO_1_3	0	I/O	General purpose I/O
		1	I/O	JTAG TDO
		2	I/O	Keyboard pin 7
		3	I	Quadrature decoder X direction input channel A
		4	O	I2S master clock output
		5	I	I2S slave clock input
		6	O	SWD SWO/JTAG TDO
16	GPIO_1_4	0	I/O	General purpose I/O
		1	I	JTAG TDI
		2	I/O	Keyboard pin 8
		3	I	Quadrature decoder X direction input channel B

Pin #	Pin name	MUX Option	I/O	Description
		4	I/O	I2S master word-select signal
		5	I/O	I2S slave word-select signal
		6		N/A
17	GPIO_1_5	0	I/O	General purpose I/O
		1	O	UART 1 RTS
		2	I/O	Keyboard pin 9
		3	I	Quadrature decoder X direction input index signal
		4	I/O	I2S master data channel 0
		5	I/O	I2S slave data channel
		6	O	ETM TRACEDATA[0]
18	GPIO_1_6	0	I/O	General purpose I/O
		1	I	UART 1 CTS
		2	I/O	Keyboard pin 10
		3	I	Quadrature decoder Y direction input channel A
		4	I/O	I2S master data channel 1
		5	I/O	I2S slave data channel
		6	O	ETM TRACEDATA[1]
19	GPIO_1_7	0	I/O	General purpose I/O
		1	O	UART 1 TXD
		2	I/O	Keyboard pin 11
		3	I	Quadrature decoder Y direction input channel B
		4	I/O	I2C 0 SCL
		5	O	PWM 3
		6	O	ETM TRACEDATA[2]
20	GPIO_1_8	0	I/O	General purpose I/O
		1	I	UART 1 RXD
		2	I/O	Keyboard pin 12
		3	I	Quadrature decoder Y direction input index signal
		4	I/O	I2C 0 SDA
		5	O	PWM 4
		6	O	ETM TRACEDATA[3]
28	GPIO_2_0	0	I/O	General purpose I/O
		1		N/A
		2	I/O	Keyboard pin 13
		3, 4, 5, 6		N/A
29	GPIO_2_1	0	I/O	General purpose I/O
		1	O	UART 1 TXD
		2	I/O	Keyboard pin 14
		3	O	Slave-select signal (SSN) 1 from SPI master (active low)
		4	I/O	Counter I/O signal 0
		5	O	Audio sigma/delta output left channel
		6	O	BLE TX enable indicator
30	GPIO_2_2	0	I/O	General purpose I/O
		1		N/A
		2	I/O	Keyboard pin 15
		3		N/A
		4	I/O	Counter I/O signal 1
		5, 6		N/A
31	GPIO_2_3	0	I/O	General purpose I/O
		1	O	UART 0 TXD
		2	I/O	Keyboard pin 16
		3	I	Quadrature decoder Z direction input channel A
		4	I/O	Counter I/O signal 2
		5	O	Audio sigma/delta output right channel
		6	O	BLE Rx enable indicator

Pin #	Pin name	MUX Option	I/O	Description
32	GPIO_2_4	0	I/O	General purpose I/O
		1		N/A
		2	I/O	Keyboard pin 17
		3		N/A
		4	I/O	Counter I/O signal 3
		5, 6		N/A
33	GPIO_2_5	0	I/O	General purpose I/O
		1	I	UART 0 RXD
		2	I/O	Keyboard pin 18
		3	I	Quadrature decoder Z direction input channel B
		4	I/O	Counter I/O signal 4
		5	O	32KHz clock signal
		6	O	BLE RX enable indicator
34	GPIO_2_6	0	I/O	General purpose I/O
		1		N/A
		2	I/O	Keyboard pin 19
		3		N/A
		4	I/O	Counter I/O signal 5
		5, 6		N/A
35	GPIO_2_7	0	I/O	General purpose I/O
		1	I	UART 1 RXD
		2	I/O	Keyboard pin 20
		3		N/A
		4	I/O	Counter I/O signal 6
		5		N/A
		6	I	Audio PDM input data right channel
36	GPIO_2_8	0	I/O	General purpose I/O
		1		N/A
		2	I/O	Keyboard pin 21
		3		N/A
		4	I/O	Counter I/O signal 6
		5		N/A
		6	I	Audio PDM input data left channel
38	GPIO_3_2	0	I/O	General purpose I/O
		1		N/A
		2	I/O	Keyboard pin 22
		3	I	WLAN Tx signal (for WIFI/BLE coexistence)
		4	I/O	Slave-select signal (SSN) 2 from SPI master (active low)
		5		N/A
		6	O	Active power domain (PD1) watchdog timer (WDT) reset signal
39	GPIO_3_3	0	I/O	General purpose I/O
		1		N/A
		2	I/O	Keyboard pin 23
		3	I	WLAN Rx signal (for WIFI/BLE coexistence)
		4	I/O	Slave-select signal (SSN) 3 from SPI master (active low)
		5		N/A
		6	O	Active power domain (PD1) watchdog timer (WDT) reset signal
40	GPIO_3_4	0	I/O	General purpose I/O
		1	O	SPI master clock (CLK) output
		2	I/O	Keyboard pin 24
		3	I	SPI slave clock (CLK) input
		4	O	BLE active signal (for coexistence)
		5	I	Quadrature decoder Z direction input index signal
		6	O	BLE TXD enable indicator
41	GPIO_3_5	0	I/O	General purpose I/O

Pin #	Pin name	MUX Option	I/O	Description
		1	I	SPI master MISO
		2	I/O	Keyboard pin 25
		3	O	SPI slave MISO
		4	O	BLE active signal (for coexistence)
		5	O	Quadrature decoder X direction LED signal
		6	O	32MHz clock (or divided down version) output
42	GPIO_4_0	0	I/O	General purpose I/O
		1	O	SPI master MOSI
		2	I/O	Keyboard pin 26
		3	I	SPI slave MOSI
		4	I/O	I2C 1 SCL
		5	O	Quadrature decoder Y direction LED signal
		6	O	Audio PDM clock
43	GPIO_4_1	0	I/O	General purpose I/O
		1	O	Slave-select signal (SSN) 0 from SPI master (active low)
		2	I/O	Keyboard pin 27
		3	I	Slave-select signal (SSN) for SPI slave (active low)
		4	I/O	I2C 1 SDA
		5	O	Quadrature decoder Z direction LED signal
		6	O	32MHz clock (or divided down version) output

3 Function Block Description

3.1 CPU and memory subsystem

The device integrates a powerful ARM® Cortex®-M4F processor core and its associated busses and memories. The Coretex-M4F processor incorporates a processor core, Nested Vectored Interrupt Controller (NVIC), high-performance bus interfaces, and a Floating-Point Unit (FPU).

This subsystem also includes two independent DMA controllers with 2 channels each, 96 KB of SRAM for data and instruction, and 256KB of ROM. Among the 96KB data/instruction SRAM memory, 16KB is used as cache memory for the XIP (execute-in-place) flash memory controller by default. The 96KB SRAM memory consists of multiple memory banks of smaller sizes, as small as 4KB. The 256KB ROM contains a boot loader and BLE 5 protocol stack.

The device also integrates a 512KB stacked flash memory for user program and data storage. The device supports XIP mode for the flash memory so that the user can directly execute the program from flash memory rather than copying it into SRAM to run.

Figure 5 and Figure 6 show the memory map in detail. The communication system in Figure 5 consists of the RF transceiver, BLE and SDR basebands, and modem. Please note that some reserved address spaces contain the Cortex-M4 's private peripherals and system controls. Users may refer to the ARM Cortex-M4 Processor Technical Reference Manual [1] for more information.

The device has integrated 4Kb of eFuse memory. The eFuse has two banks: the vendor bank and the customer bank. The vendor bank stores the device's UUID, product type number and transceiver calibration parameters. Users can use the customer bank to store their application

dependent data. Once the eFuse memory is programmed and locked, the content of the eFuse memory will become permanent and cannot be modified or changed.

Active power consumption of the Cortex®-M4F is 45uA/MHz at 3.0V as chip supply voltage with the built-in buck converter enabled and 1.2V as core supply voltage.

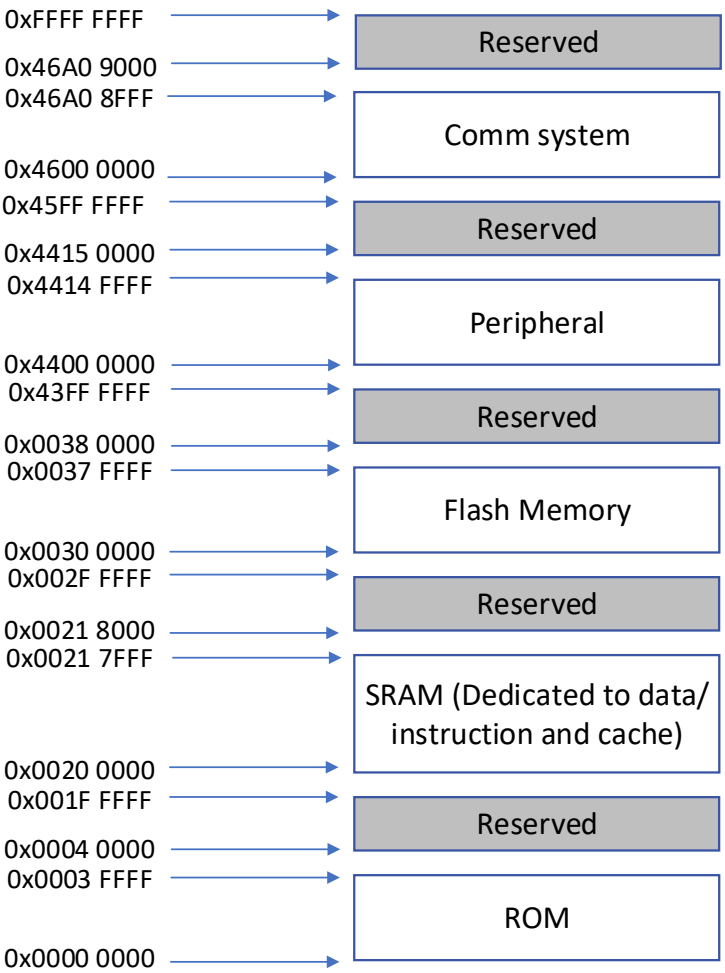


Figure 5: Memory map

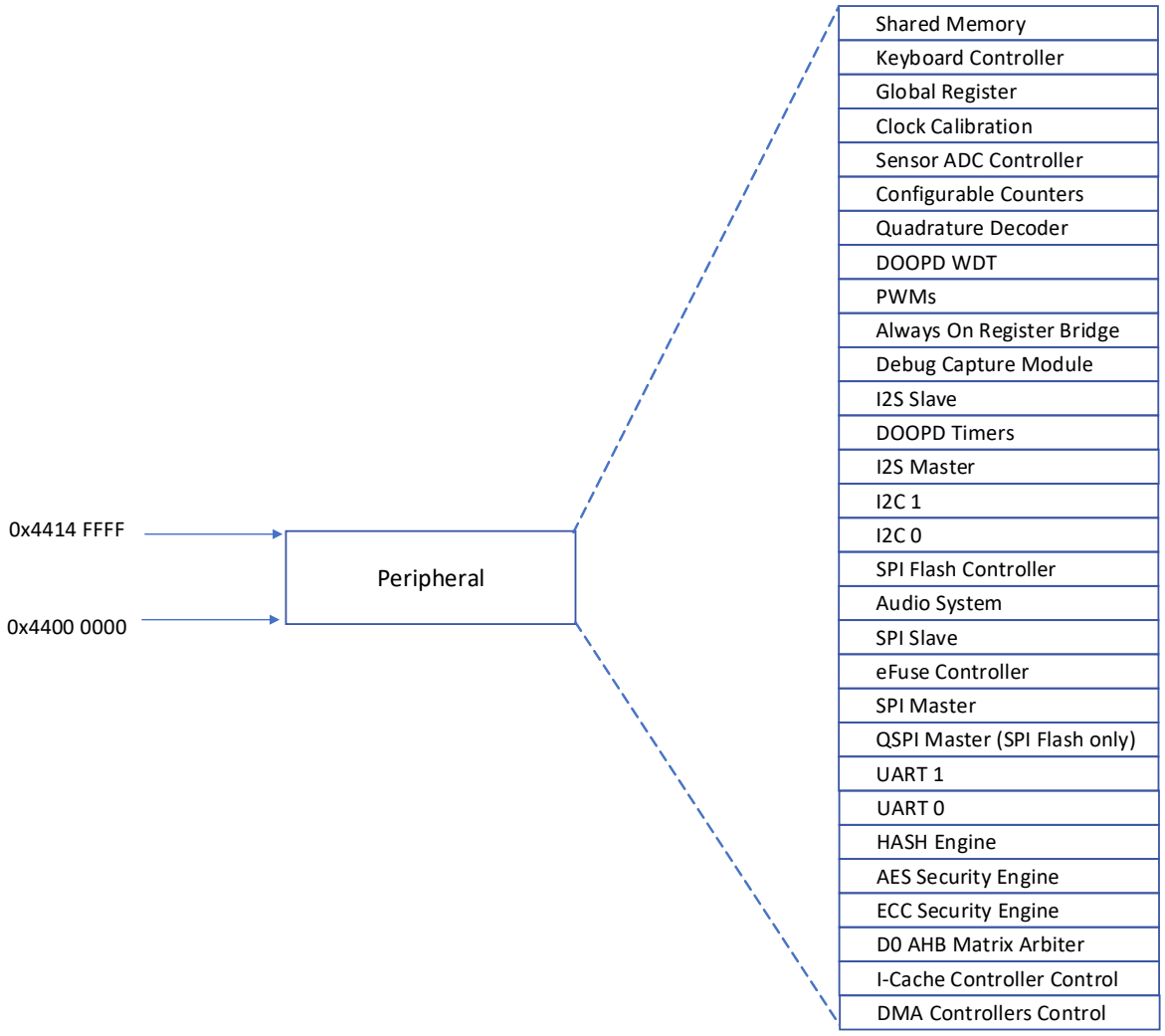


Figure 6: Peripheral memory map

3.2 Power system and clocks

3.2.1 Power supplies

Figure 7 shows the power architecture. The device needs four external power supplies including VBAT, VDDIO1, VDDIO2, and VDDQ.

- VBAT is the chip power supply.
- VDDIO1 and VDDIO2 are the I/O power supplies.
    - GPIO_0_X, GPIO_1_X pins are in the VDDIO1 domain.
    - GPIO_2_X, GPIO_3_X, GPIO_4_X and TEST_MODE pins are in the VDDIO2 domain.
- The VDDQ is the eFuse memory programming supply. During the eFuse programming, the VDDQ voltage must be present and be in the range of 3.3V±10%. During other operations, the VDDQ is not needed.

Inside the device, it has a step-down DCDC converter, an AONPD (Always-ON Power Domain) LDO, a retention LDO, and two VDDIO switches.

- The AONPD LDO (also called AON LDO or PD0 LDO) is automatically enabled by hardware once the chip is enabled. The AONPD logic is powered by this LDO.
- The DCDC powers the RF transceiver (by routing the VDD_DCDC pin externally to pins VDD_VCO_2G4, VDD_RF_2G4, VDD_PLL, VDD_AMS on the PCB) and the digital core including the CPU, BLE modem and baseband, SDR modem and baseband, security engines, peripherals etc. and eFuse memory through a digital core LDO.
- The memory banks are powered by the digital core LDO in active operation mode and by the retention LDO in deep sleep mode when they are configured to be retained.
- The VDDIO switch1 (VDDIO SW1) provides power to the stacked flash memory through VDDIO1 inside the QFN48 package. In deep-sleep mode, the switch can be turned off to reduce leakage power.
- The VDDIO switch2 (VDDIO SW2) can be used to provide power to external sensor through VDDIO2. In deep-sleep mode, the switch can be turned off to reduce leakage power. VDDIO SW2 is not bonded out on the QFN48 package.

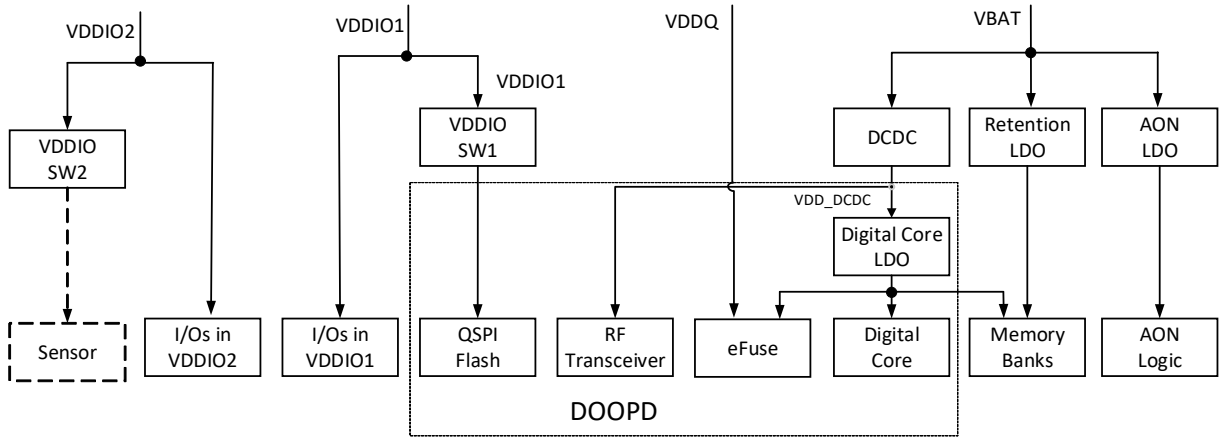


Figure 7: Device power supplies

3.2.2 Power sequence

The CHIP_EN pin can be used to enable and disable the device. A "high" (>=0.7*VBAT) on the CHIP_EN pin would enable the device, and a "low" (<=0.3*VBAT) would disable the device. Figure 8 shows the desired power-up sequence. The rising time for CHIP_EN should be less than 5ms.

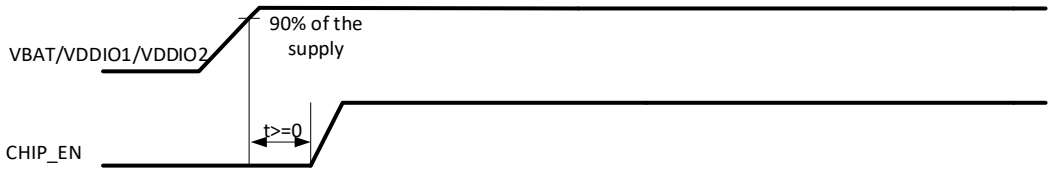


Figure 8: Power-up sequence

To reset or re-enable (temporarily disable and re-enable) the device in the middle of operation, customer may toggle the CHIP_EN pin and hold the CHIP_EN at "low" for at least 100 us as shown in Figure 9. The rising time for CHIP_EN should be less than 5ms.

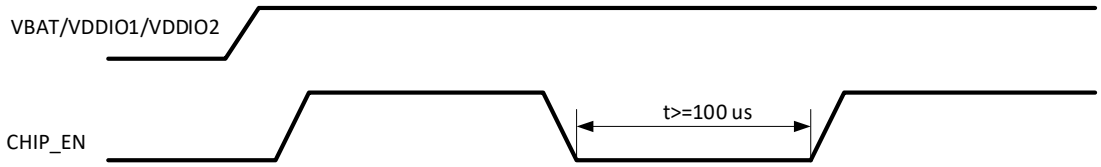


Figure 9: Reset the device (Re-enable the device)

3.2.3 Power domains and power operation modes

The power supply system ensures the correct timing and voltage for each operating mode or block. The device has the following power domains:

- AONPD (Always-On Power Domain, also called as PD0 or AON domain).
  - Once the device is enabled, this domain is always powered.
  - This domain uses clocks generated from low frequency oscillators.

  - This domain has multiple sleep timers and sleep/wakeup control, and control for the power and clock management unit.
  - The supply to this domain the AONPD LDO.
- DOOPD (Dynamic On-Off Power Domain, also called as PD1):
  - All the logic blocks expect those in PD0 belong to DOOPD, which include CPU, peripherals, transceiver, BLE and SDR baseband and modem, the majority of Power Management and clock Unit (PMU), security engines, eFuse memory, and flash.
  - The main clock used in this domain is generated by high frequency oscillators in the PMU.
  - The main supply to this domain is the DCDC and the digital core LDO. The flash is powered by VDDIO1.
  - The supplies to DOOPD can be turned off and on, depending on the power modes.
- 12 memory banks (including 7 data/instruction memory banks and 5 shared memory banks):
  - The supplies to these memory banks are the digital core LDO and the retention LDO,
  - The memory banks can be in active, retention, or power-down mode.

The device has three main power modes:

- **Chip active mode**:
  - All power domains are on. Upon the power-up, the device enters the active mode. Powers to all internal blocks are turned on. The user can use software to let the chip go to deep sleep mode.
- **Chip deep sleep mode:**
  - The power (provided by the AONPD LDO) to the AONPD domain is on.
  - Only the low frequency clocks for the AONPD are on, and the high frequency clocks are turned off.
  - The registers on the AONPD are retained. These registers are called AON registers.
  - The power (provided by the retention LDO) to the data/code memory and shared memory banks is user configurable by software, prior to the device entering deep sleep mode.
  - The DCDC and digital LDO are disabled, which are the power supplies to DOOPD.
  - The supply to the stacked flash is turned off (VDDIO SW1 is turned off in Figure 7).
  - In this mode, sleep timers and BLE events (user and application configurable) can decide when to wake up the device to enter the active mode. The external signals on GPIO pads or a brownout detection event can also wake up the chip.
- **Chip off mode**:
  - All internal power supplies (including DCDC, digital core LDO, retention LDO, AON LDO) are disabled, and all internal blocks are powered off, and all clocks are turned off. The leakage current in this mode is less than 20nA. To enter this mode, the CHIP_EN needs to be brought to "low". To exist this mode, the CHIP_EN needs to be pulled to "high".

3.2.4 Cold boot and warm boot

Throughout this document, the process from the chip off mode to the chip active mode is called **cold boot**. The process from the chip deep sleep mode to the chip active mode is called **warm boot**.

3.2.5 DCDC converter

The buck DCDC converter, as shown in Figure 10, efficiently reduces the voltage of the chip main supply (VBAT) to around 1.2V. The 1.2V supply is used to power the radio transceiver directly. In addition, it is used as the input to an LDO that in turn creates the supply for the digital core. Two external components are required for the DCDC converter, an inductor, and a capacitor. The recommended values are 10uH and 1uF, respectively. Other values are permitted; however, they will affect the behavior of the DCDC in terms of efficiency, startup time, and ripple amplitude.

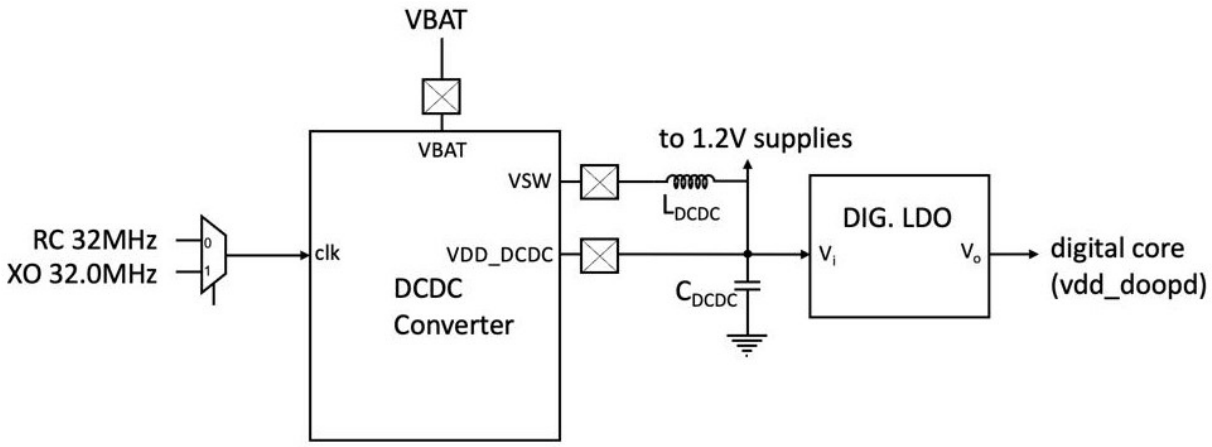


Figure 10: DCDC buck converter

3.2.6 Clock system

The device's clock system is designed to provide clocks to all subsystems that require clocks and for switching between different clock sources without degrading system performance or power consumption.

There are five types of clock sources. They are RC 32kHz, RTC 32 kHz, RC 32MHz, XO32/64MHz, and programmable CLK from the clock PLL. The RC 32KH and RC 32MHz are generated internally. The RTC 32 kHz and XO 32/64MHz need external crystal oscillators. The user can also inject the RTC 32.768 kHz or 32 kHz clock to the device. The clock PLL is used internally for the transceiver.

Different clocks (and their divided down versions) are used in different clock domains. The high frequency clocks (RC 32MHz and XO 32/64MHz clocks) can be used as the root clock of the logics in the DOOPD, as illustrated in Figure 11. The DOOPD logics are divided into three clock regions. All peripheral interface logics on the CPU system bus (including I2C, UART and other modules) are in the clock domain 0 (D0). The communication related logics, including BLE and SDR baseband and modem, are in the clock domain 1 (D1). The Cortex-M4 CPU, its memories and instruction cache

(iCache) are in the clock domain 2 (D2). The low frequency clocks (RC 32kHz and RTC 32 kHz) can be used as the root clock of AONPD.

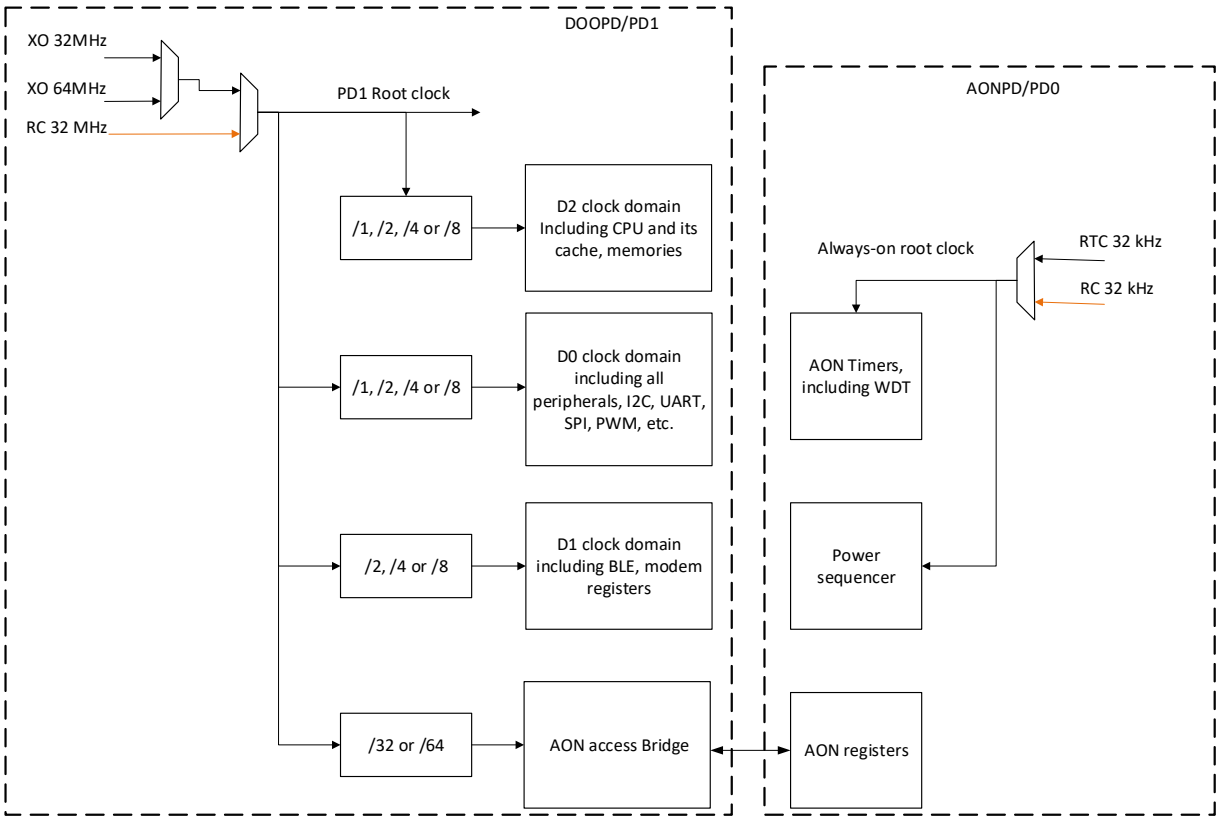


Figure 11: Root clocks and clock domains

3.2.5.1 RC 32kHz

The RC32kHz clock is a low-frequency clock generated internally for the AONPD logic. This clock is automatically enabled by hardware once the chip is enabled, and is the default clock source for the AONPD after cold boot.

3.2.5.2 RTC 32kHz

For applications where high accuracy for low-frequency clocks is needed, the user can install a 32 kHz or 32.768 kHz external crystal oscillator, as illustrated in Figure 12. To save BOM, the device provides a programmable on-chip load capacitance, up to 16 pF, for the external crystal oscillator. The device also supports an external 32/32.768 kHz clock source as input as shown in Figure 13.

The RC 32kHz is the default clock for the AONPD logic, upon cold boot. The switching from the internal RC 32kHz to the external RTC 32 kHz is software configurable.

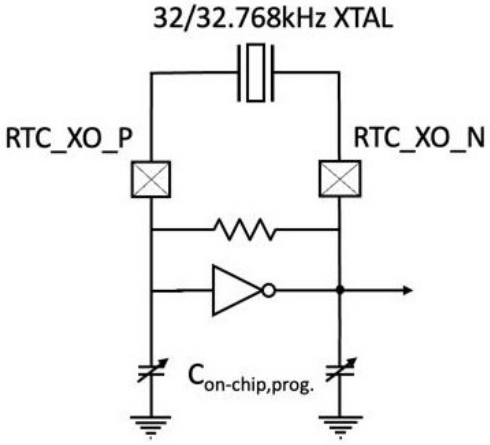


Figure 12: 32/32.768kHz crystal

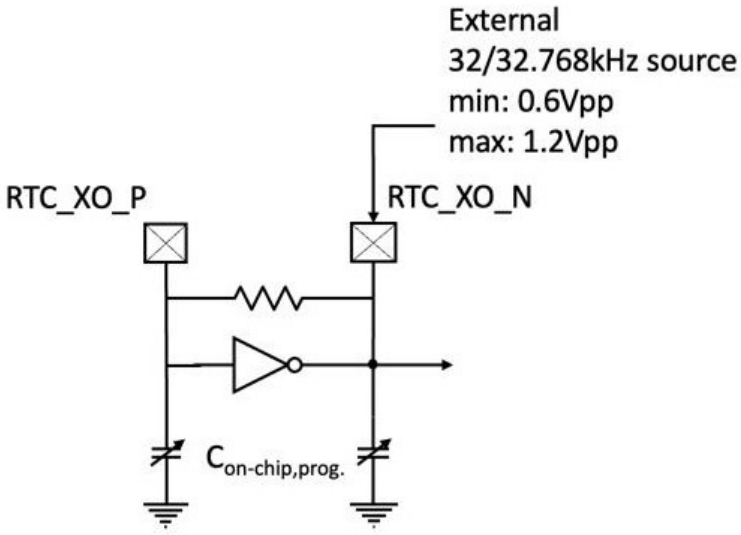


Figure 13: External 32/32.768kHz source

3.2.5.3 RC 32MHz

The RC 32MHz is generated by an internal 32MHz high-frequency ring oscillator that provides a clock to the DOOPD. This RC 32MHz oscillator is automatically enabled by hardware once the chip is enabled. The root clock to the DOOPD is the RC32MHz up a cold boot or warm boot. The switch from the RC 32 MHz clock to XO clocks is software configurable.

3.2.5.4 XO clocks (XO 32MHz and XO 64MHz)

The XO clocks (XO 32MHz and XO 64MHz) are high-frequency clocks. To generate these clocks, the user needs to install an external 32 MHz crystal oscillator as shown in Figure 14. The XO clocks are controlled by AONPD and are enabled by default after a cold boot. There is software programmable on-chip load capacitance, up to 8 pF for the external crystal oscillator. Besides, the 32 MHz clock

(XO 32MHz), the XO circuitry also includes an XO doubler (XOX2) which generates the 64MHz clock (XO 64MHz or XOX2).

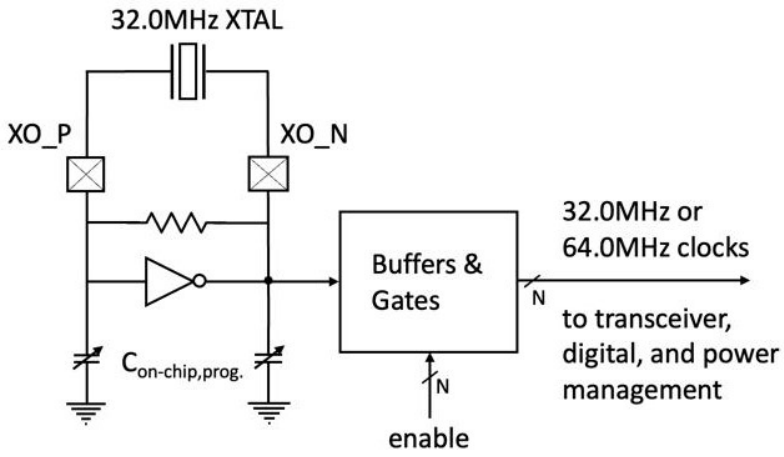


Figure 14: XO clock source

3.2.5.5 CLK PLL

The Clock PLL is designed to provide multiple clock frequencies for different clock requirements for the radio transceiver on different PHY rate receptions. By default, the clock PLL is automatically controlled by the hardware.

3.2.7 BOD (Brown-Out Detection)

The device supports brown-out detection with four programmable thresholds. The BOD monitors the voltage of the chip main supply (on VBAT pin). If the voltage is below the threshold that the user has programmed, the BOD can trig interrupt. The user can also use the BOD trigger to reset the device. For more information, see the Reference Manual.

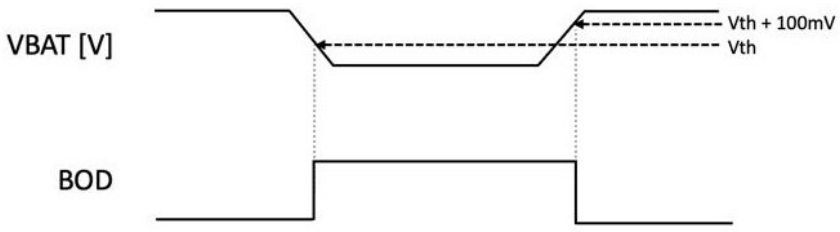


Figure 15: BOD input and output waveforms.

3.3 BLE 5 radio and subsystem

The device incorporates a Bluetooth® low energy (BLE) subsystem that contains the physical (PHY) and link layer engines with an embedded security engine and is fully compliant with Bluetooth® core 5 specifications including all the optional features supported such as extended advertising packet length, higher throughput, and long-range mode.

The device supports 1Mbps and/or 2Mbps PHY rates over 2.4GHz ISM frequency bands. It can also support long-range mode to transmit and receives either 500Kbps or 125Kbps modulated packets.

The baseband controller combines both hardware and software implementation that supports all device roles (broadcaster, central, observer, and peripheral). The timing critical functions are implemented in hardware such as encryption/decryption, FEC decoder, CRC, data whitening, and access address detection.

Key BLE5.0 features being supported are as followings:

- Bluetooth® low energy v5.0 specification compliant
- All PHY rates are supported including 1 & 2 Mbps, 125 & 500 kbps.
- Packet length up to 255 bytes
- Encryption/decryption (AES-CCM) for enhanced security at the link layer
- Bitstream processing (CRC, whitening)
- All device roles support (broadcaster, central, observer, and peripherals)
- Backward compatible to BLE v4.0/4.1/4.2 features.

The 2.4GHz transceiver has one chip pin, RF_TRX_2G4, for both the transmission and reception of RF signals, as shown in Figure 16. An on-board matching network is recommended to get the best RF performance out of the device. The matching network can favor the RX path over the TX path or vice-versa, but the recommended matching network in the reference design is a balance of both paths. There are four supply pins for the 2.4GHz transceiver, which are nominally 1.2V. They should normally be connected to the DCDC output, VDD_DCDC. The transceiver needs a 32.0MHz crystal oscillator reference. To reduce BOM cost, the capacitor for the crystal is integrated on-chip. The on-chip load capacitance can be programmed from 0.5 pF to 8 pF in 0.5 pF steps.

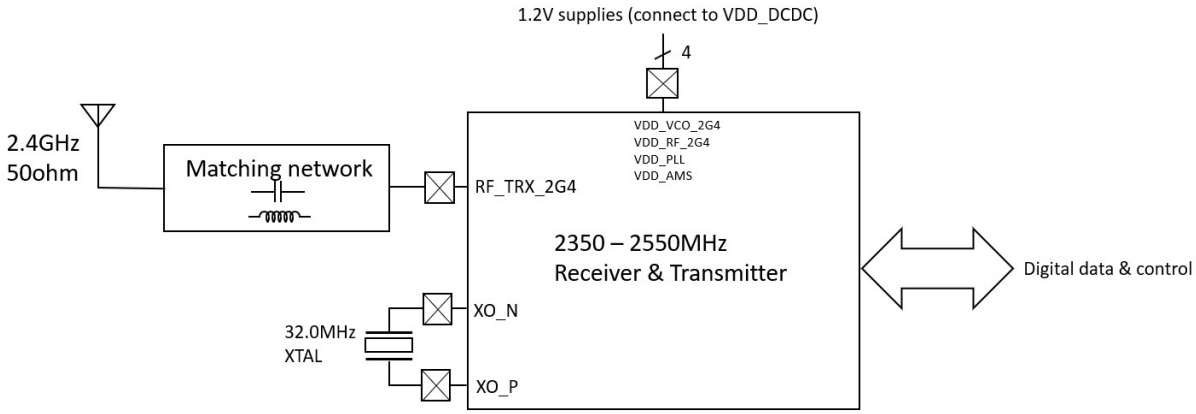


Figure 16: 2.4GHz RF transceiver

3.4 Software-defined radio

The device incorporates a software-defined radio (SDR) with which users can develop a wireless communication network with their proprietary protocols. The SDR supports GFSK modulation with up to +3dBm as TX power output (2.4 GHz). Also, multiple data rates can be selected among 125 kbps, 500 kbps, 1 Mbps, and 2 Mbps.

- Event-driven and event-based communication:
  - The data communications among the devices have one or multiple events, as shown in Figure 17. Two roles are defined for InPlay® SDR devices: initiator and responder. The device that first starts transmission in an event is called an initiator. The device that always starts from reception is called a responder. The roles of a device can be freely configured by software for different events as shown in Figure 17.
  - The initiator can be very low power. Most of the time, it can be in sleep or idle states. Only when there is a need, the software can program it to start an event.
- BLE 5.0 and SDR coexistence
  - The device supports BLE and SDR coexistence.
- Connectionless data communication
  - It is not required for the two devices to be connected before data communication.
- Multiple TX and RX during an event enable high-throughput communication
  - During an event, multiple transmissions and receptions are supported as shown in Figure 17, which allows multiple packets exchanged between the initiator and the responder.
- Multiple hardware interrupts to facilitate software real-time processing.
  - SW programs a device to start an event for data communication. During an event, RX and TX interrupts will be generated once a packet is transmitted or received. In the end, an end-of-event interrupt will be generated. These interrupts can be used by software for real-time processing.
- Easy software handling
  - The software can start an event at any time if there is no overlap. Once an event starts, the hardware state machine takes over the transmission/reception process. If there is no more data packet to be exchanged or is a timeout, the hardware will automatically terminate the event.
  - An event can be also terminated or canceled by software by just setting a register bit.
- Broadcast
  - A device can send out broadcasting packets to all other devices.
- Private communication with the source address and destination address
  - In a network, each InPlay SDR device can be assigned a 16-bit address which allows private communication between two devices.
- Low latency and fast response
  - For each event, a responder can prepare and program multiple sets of TX packets. Each set has multiple TX packets, and each set is targeted to a specific initiator. Once a responder receives a packet from an initiator, it will perform an address match automatically and pick the corresponding set of TX packets to communicate to the initiator. This feature enables low-latency and fast response communications. If there is no address match, the responder will simply respond with a packet without payload.

- During an event, if a responder receives a packet whose destination address does not match the responder's address, the responder will simply ignore that packet and continue to be in reception mode.

- BLE and SDR coexistence
  - The device supports BLE and SDR coexistence by flexing hardware and software tools.

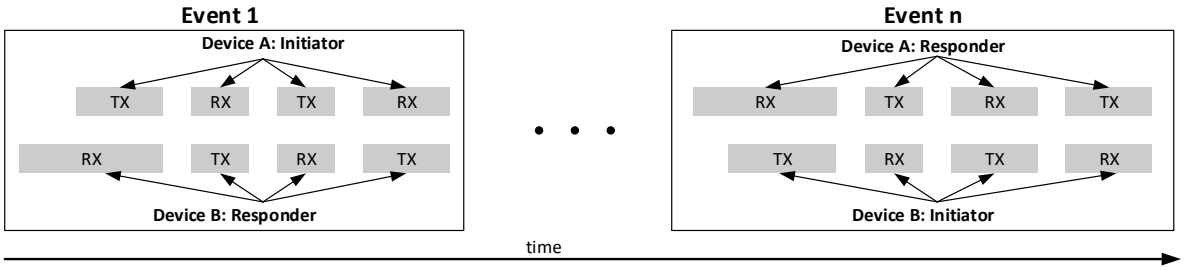


Figure 17: SDR event and roles

3.5 Arbitrary format TRX

The device supports a flexible transmission and reception which we call arbitrary transmission. The corresponding baseband is called arbitrary transmission BB (ATBB) where the software can control the transmitting packet format. Figure 18 shows the packet format of the ARBB. The content of the sync pattern (also called access address) is defined by the software. In addition, the software fully controls the content and length of the header, payload, and CRC.

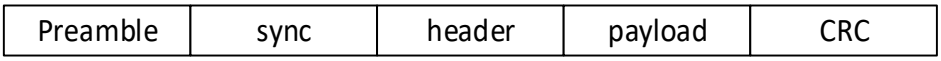


Figure 18: Packet format for arbitrary TRX

On the receiver side, the SW just needs to specify the expected sync pattern. Once it receives a packet with the expected SYNC pattern, the receiver will signal to the CPU.

The channel and PHY rate are also fully programmable and controlled by the software. Two PHY rates (1Mbps and 2Mbps) are supported.

The arbitrary TRX format enables users to fully control the RF transceiver and develop their protocol stack.

3.6 Special function blocks

3.6.1 11-bit sensor ADC

The device has a sensor ADC block as shown in Figure 19 which the user can use for converting analog signals to digital domain signals for CPU processing. The input signal to the Sensor ADC is a single-ended voltage.

The sensor ADC has 11 physical bits and can convert at a maximum of 64 KSPS. The actual clock speed and conversion rate are controlled by software. The input to the ADC is preceded by a multiplexer (the multiplexer has 16 inputs, but 4 of them are grounded or reserved for chip testing) which enables the user to sample up to 12 different channels (package option dependent). One of the 12 channel is a dedicated sensor ADC input (ADC_IN pin); nine are from mixed-signal GPIO pins (GPIO_2_X pins). In addition, the ADC can be used to measure the voltage level at the VBAT pin or the temperature. The digital control system for the ADC gives the user the flexibility to choose which channels are sampled in what order. The required voltage reference (VREF) is from an on-chip 1.0V reference. The input voltage range to the ADC shall be between 0V and 2*VREF, i.e., between 0 and 2V.

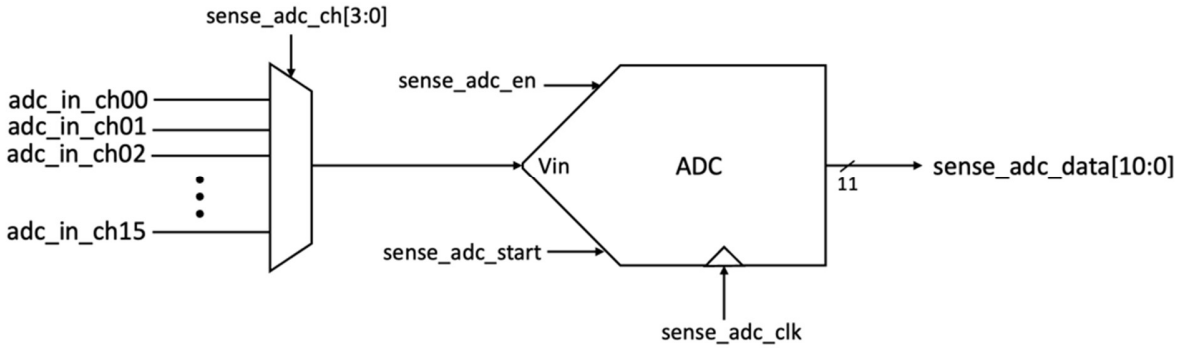


Figure 19: Sensor ADC

3.6.2 Hardware security engine

The device integrates a set of security and cryptographic engines which comprise of hardware accelerators for AES, SHA, and ECC algorithms. These engines/accelerators are open to user applications.

The AES module implements the AES encryption and decryption algorithm as defined by the NIST FIPS Publication 197. The features supported by this block are:

- Configurable key lengths of 128, 192, and 256 bits.
- XCBC, F8, CMAC, CCM, CBC, CTR, and ECB modes are supported.

The SHA module implements the HASH algorithm and supports SHA-1 and SHA-2.

The ECC module contains the accelerators for integer operations (such as modular exponentiation) and ECC point operations which can be used by software to implement various ECC algorithms. The ECC key lengths supported are 160, 192, 224, and 256 bits. The key length and the ECC curve are configurable by software.

Besides these mentioned engines, there is a dedicated AES engine used by the BLE baseband and controlled directly by Bluetooth Low Energy protocol SW stack.

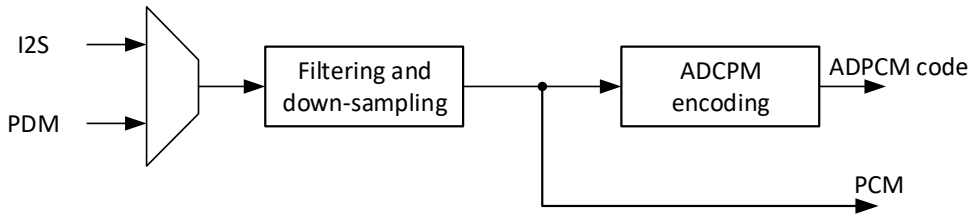
The device has a true random number generator (TRNG) which is based on thermal noise. It is accessible to user applications.

3.6.3 Audio ADPCM and resampling engines

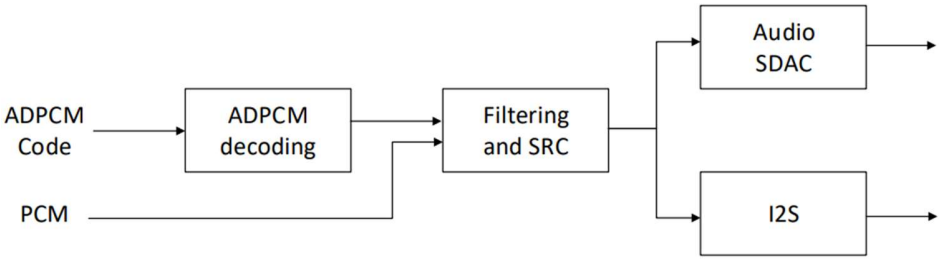
The device has ADPCM and audio sampling rate conversion (SRC) engines which can be used to support and develop wireless voice and audio applications.

The audio engine takes the audio data input from either PDM or I2S interface. The input audio data can be encoded with ADPCM or directly output with 16-bit PCM format to the radio interface as shown in Figure 20(a).

The audio engine can also take the PCM or ADPCM data (wireless received from a remote device) as input. It converts them to the desired format and sends the processed audio data to the sigma-delta DAC (SDAC) or I2S interfaces as shown in Figure 20 (b).



(a) ADPCM encoding and PCM output



(b) ADPCM decoding and PCM input.

Figure 20: Audio engines

3.6.4 Keyboard controller

The device has a keyboard controller module that scans through the columns or rows to identify each key's row/column index.

Users can define the scan interval and scan through all columns/rows every 0.5, 1, 2, or 4 milliseconds. Every time after the scan, if any key status has been updated, an interrupt will be

generated to the CPU. At the same time, the following information will be stored in the status registers:

Table 4: Key information register format

1 bit (press/release)	1 bit (multi-key event)	28 bits (row/column index) of the key

The first bit indicates if the key is pressed or released during the scan. The second bit indicates if the multi-key event happens (used to support multiple keys pressed/released at the same time). If this bit is asserted, the second status register (same format as the first one) will be populated. If this bit in the second register is also set, the third register will be populated, and so on. At most 4 key status registers will be stored. The last field in the registers is used for the column/row index of the key. The number of GPIOs used for columns and rows can be configured through control registers. The number of regular keys and special keys (such as shift, control, alt, home, end, etc.) can be configured through the control register and the maximal number of supported keys is 108.

Based on the control registers setting, the de-bouncing filter can filter out glitches up to 63 milliseconds (in the step of 1 ms). The press and release de-bouncing filter can have different filtering time values.

3.6.5 Quadrature decoder

The device has a quadrature decoder with which the users can interface the device to a mechanical or an electronic rotary device such as a servo motor, volume control wheels, PC mice, etc. The decoded quadrature signals are used as data input to the system to determine the absolute or relative position of the rotary device.

The quadrature decoder comprises channel A, channel B and LED signals as interface pins to the external rotary device. Channel A and channel B are input signals from the external quadrature encoder to indicate the movement of the rotary device. The LED signal is an optional output signal to the external quadrature encoder and will be asserted a few microseconds (defined through control registers) before the sampling and de-asserted immediately after the channel A and channel B values are sampled by the decoder.

An optional de-bounce filter can be enabled. The channel A and channel B values are only valid if their values are constants during the de-bounce filter window (which is the same length as the sampling interval). If there is a short-time glitch on channel A or B within the de-bounce filter window, the glitch will be ignored. When the de-bouncing filter and LED signal are enabled, the LED will stay asserted during the de-bouncing filter window.

3.7 Peripherals

3.7.1 I2C

I2C is a simple two-wire bus with a software-defined protocol for system control and peripherals. It has serial data (SDA) and serial clock (SCL) interface signals. The device has two independent I2C interfaces. The maximum I2C clock rate supported is 1MHz.

I2C can be configured to operate in either master or slave mode. The user has the flexibility to determine and program the slave I2C address. It uses 7-bit addressing. It supports bulk transmit mode.

The I2C has access to the DMA Controller and the data can be transferred between CPU memory and the I2C data buffer through the DMA.

3.7.2 SPI

SPI is a four-wire serial peripheral interface bus commonly used to send data between the microcontroller and peripherals. It comprises a clock (SCK) and data lines (MOSI and MISO) along with a slave select (SS) signal.

The device has one SPI master interface and one SPI slave interface. In the master interface, the maximum clock rate supported is 16MHz. In the master mode, the device can support up to 4 independent slaves using different SS signals while sharing the same SCK, MOSI, and MISO signals.

In the slave mode, the device can operate on the SCK clock rate up to 8 MHz.

SPI has access to the DMA controller and the data can be transferred between CPU memory and SPI data buffer through the DMA.

3.7.3 QSPI

The device has a QSPI master which is dedicated to the access of the stacked flash. The maximum clock rate is 32MHz. The interface is not bonded out.

3.7.4 UART

The device includes two UART cores which support universal asynchronous transmitter/receiver function and support programmable baud rates up to 2 Mbps.

The UART has built-in 16 bytes of transmit and receive data FIFO and supports auto flow control. The UART has access to the DMA controller and the data can be transferred between CPU memory and UART data buffer FIFO through the DMA.

3.7.5 Counter/timer/PWM

The device has 6 32-bit timers that run on the 32MHz XO clock (or divided version of the 32MHz), 2 32kHz 32-bit timers, and 4 flexibly configurable counters in the active power domain.

The 4 flexibly configurable counters can be used to capture values (and the time duration) of the external slow signals. They can also be used to send signals out based on the configuration registers. They can be used for infrared remote control (including learning and transmitting) and can be configured to support ISO-7816 protocol signals. They can also be used for other features such as frequency estimate of external signals, clock generation, timing delay, etc. They can also be chained together to create more complicated signals.

The device has two timers in the always-on (AON) power domain. Both can be used by the user for implementing timer functionality in a lower-power fashion without waking up the CPU. The clock source for the timers in the AON power domain can be either an internal RC 32kHz clock or an external RTC 32.768kHz clock. A watchdog timer is also available in the AON power domain.

The device has five pulse width modulation (PWM) modules with programmable output frequencies and duty cycles. The clock source can be from 2MHz up to 32MHz which provides a high-resolution output frequency.

3.7.6 PDM

The device has a PDM interface that can convey audio data digitally over a CLK (clock)/PDM (PDM bit stream) pair. The device supports both mono stream and stereo stream of input from an external PDM peripheral with multiple PDM clock rate support from 160kHz to 5.12MHz. The PDM bit stream is clocked at a single edge (selectable) for mono stream or clocked at both edges for stereo stream. After filtering and down-sampling, a 16-bit PCM stream will be generated which can be further converted to the 4-bit ADPCM format.

3.7.7 I2S

The I2S bus is a simple three-wire serial bus protocol used for connecting digital audio devices. It includes bit clock (SCK), word select (WS), and serial data (SD) signals. It supports operating on either master or slave mode. In master I2S mode, the WS rate supported is 7.8125kHz, 8kHz, 15.625kHz, 31.25kHz, and 46.875kHz. The WS rate by default is 15.625kHz. The clock rate of SCK ranges from a few hundred kHz to 3.2MHz.

Either I2S master or slave core supports bi-directional data transfer. The I2S master supports 2 concurrent stereo channels while the I2S salve supports one stereo channel.

The I2S cores have access to the DMA controller and the data can be transferred between CPU memories and the I2S data buffer through the DMA.

3.7.8 Cache and execution-in-place (XIP)

The chip provides a 2-way set associative instruction cache capability for the stacked SPI flash to reduce the potential latency due to slower speed on the SPI interface. The cache can support up to 2M bytes of the SPI flash address space.

3.7.9 DMA

The chip provides 2 independent DMA controllers, and each controller connects to 12 different peripheral interfaces. Each controller also provides 2 parallel channels which can be enabled simultaneously. The DMA controllers support data transfer between peripheral buffers and CPU data memories.

3.7.10 WDT

Two watch dog timers (WDT) are provided in the device. One WDT is in the AON power domain, and it runs with the 32 KHz RC or RTC clock when the chip is in active or sleep mode. The other WDT is in the DOOPD (PD1) power domain, which only runs in the active mode. The DOOPD WDT runs with the divided down clock of the DOOPD root clock. The DOOPD WDT will be automatically reset (includes its configuration, counting states, and output) when the chip is in sleep mode.

The timeout signal of the AON WDT can trigger an interrupt to the Cortex® M4 CPU and its delayed version can be used to reset the chip. The timeout signal can also be sent out to a GPIO pin for external hardware logic.

The timeout signal of the DOOPD WDT is connected to the Cortex® M4 non-maskable interrupt (NMI). The second timeout signal from WDT can also be programmed to be sent through chip pins (polarity programmable) for external hardware logic to reset the chip. It can also be sent out as a periodic waveform as preprogrammed through the PWM block. The same signal can also be programmed to reset the DOOPD logic or the whole chip.

3.7.11 GPIO and mixed-signal IOs

The device supports up to 30 GPIOs (package dependent) and a dedicated analog input pin (package dependent). There are two types of GPIOs: mixed signal GPIOs and digital general-purpose IOs. A mixed signal GPIO can be configured as a digital GPIO or be configured as an analog signal input pin to the sensor ADC. The mixed GPIOs are default as digital GPIO after cold boot.

Each GPIO has a programable pullup or pulldown resistor when it is in digital input mode and has a 2-level programmable output driving strength option.

Each GPIO can be configured as a wakeup pin, and the polarity of each wakeup signal can be programmable to "high" or "low".

The device supports GPIO state retention during sleep.

All GPIOs support asynchronous interrupts. They can be configured as interrupt sources to the ARM core. Multiple GPIOs inputs are grouped to form a single interruption. For each GPIO's input, we can configure its polarity and its mask.

When the chip enable (CHIP_EN) input pin is low, the device is in shutdown mode and all the GPIOs are in the high-Z state. When the chip is enabled, all the GPIOs are in input mode by default (with pull-up enabled). After boot, the software may program the GPIOs into appropriate modes (such as input/output/high-Z state or analog input).

3.8 Emulation and debugging interface

The device integrates the Serial Wire JTAG Debug Port (SWJ-DP), which is the standard CoreSight debug port that combines JTAG and SWD debug ports. The device also supports trace functions.

Note that SWD and JTAG can be disabled if a specific eFuse bit (the JLINK disable bit) is programmed to 1, and there will be no access allowed by external debugging tools.

3.9 Flash programming interfaces

For the flash programming, the device supports JLINK programming as well as in-system programming (ISP) through UART and SPI. The ISP through UART and SPI is through the boot loader. Certain IN6XX devices with a special ROM mask do not support ISP. Please refer to Table 20 for details.

3.10 User IP protection and secure boot

Often, for a system with flash memory, there are two concerns. The first concern is how to protect the IPs in the flash memory. To protect IPs in the flash memory, one of the popular approaches is to encrypt the code. The second concern is that we need to make sure the image on the flash is an image of authenticity. To resolve the authenticity concern, secure booting is required. The device integrates a bootrom which supports flash encryption and secure boot which can be used to protect the user's IP and authenticate the image before it is executed with the help of the security engines and accelerators.

3.10.1 User IP protection

The device supports secure file transfer and flash encryption, as shown in Figure 21.

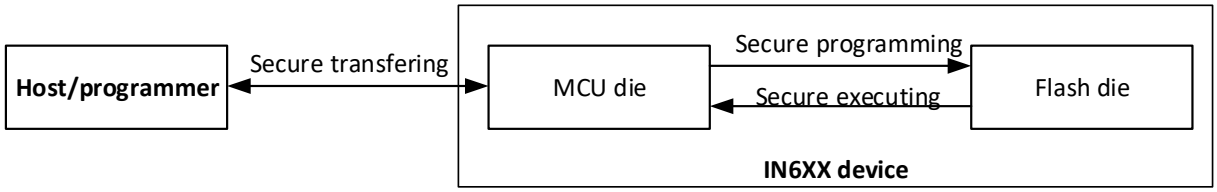


Figure 21: Secure software copyright protection

3.10.1.1 Secure transfer

The device's bootrom supports In-System flash Programming (ISP) through UART or SPI. When a programmer attempts to program the device's flash memory, the programmer and the device's boot ROM can negotiate a shared key through the Elliptic Curve Diffie-Hellman (ECDH) key exchange protocol. The key can then be used to encrypt the firmware image file as the programmer transfers it to the device. The encryption is based on AES-256. The device decrypts the firmware from the programmer and stores the image to the flash. This process is called secure transfer, it can prevent a third party from copying the IP by probing the UART or SPI connection between the programmer and the device. Secure transfer is not supported for the flash programming through JLINK interface.

3.10.1.2 Flash encryption

The firmware image file stored on the flash memory can be configured to be encrypted or unencrypted fashion. Two types of flash encryption are supported: One is AES-256 encryption. When executing the AES-256 encrypted code, the bootrom will first decrypt the encrypted code using a secret key generated by hashing the device's UUID and production definition configuration stored in the eFuse and put the decrypted code on the device's internal RAM.

Another type of encryption is InPlay's proprietary real-time encryption (PRTE) which can decrypt the encrypted code on real-time execution through XIP. An encrypted image can be configured to be partly AES-256 encrypted and partly InPlay's PRTE encrypted. The encryption keys are tied to hash digest of the device's UUID and production definition configuration by a proprietary hash engine. The same encrypted image cannot be executed on two different devices, as different devices have different UUIDs.

3.10.2 Secure boot

The device supports secure boot based on the Elliptic Curve Digital Signature Algorithm (ECDSA). To support secure boot, a firmware image is signed using ECDSA, and the resulting digital signature is attached to the firmware image, as shown in Figure 22. During cold boot, the bootrom verifies the signature. If the verification fails, the bootrom exits the boot process.

As shown in Figure 22, at the manufacturing side, a pair of ECSDA keys (private and public keys) is first created. The hash digest of the firmware image is computed. Then the hash digest and the private key are used by ECDSA to generate a digital signature. The signature is attached to the image, and is programmed to the flash. The public key is programmed to the eFuse memory, the eFuse memory can be configured to lock the public key so that it can no longer be modified or altered.

During cold boot, the boot ROM calculates the hash digest of the image on the flash. After that, the bootrom uses the ECDSA algorithm to verify the signature stored in the flash based on the public key and the hash digest. If the verification passes, the bootrom will continue to execute the image. Otherwise, it will stop the booting.

The device uses SHA-2 and ECC curves secp256r1 for the secure boot.

Certain IN6XX devices with a special ROM mask do not support secure boot. Please refer to Table 20 for details.

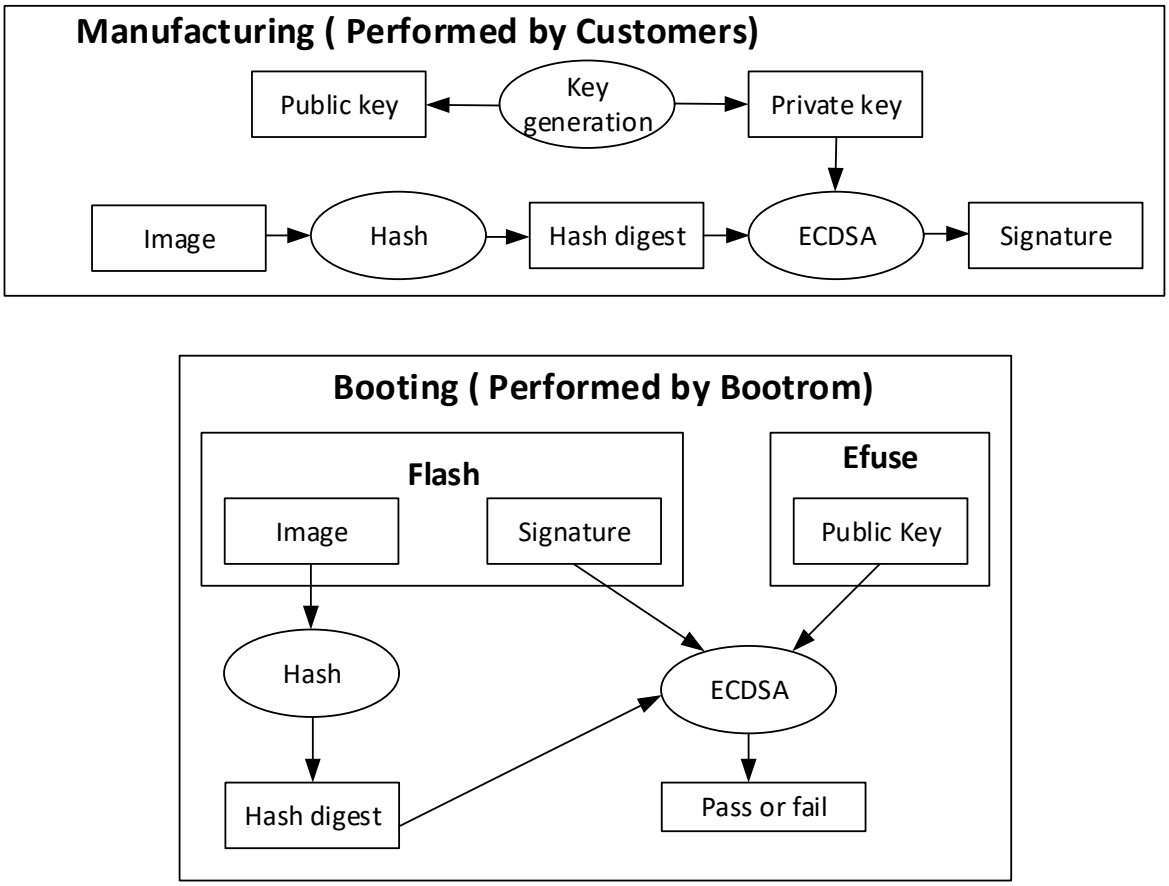


Figure 22: Secure boot

4 Electrical Characteristics

4.1 Absolute maximum ratings

The values listed in this section are the ratings at which the chip can peak, and stresses listed above the absolute maximum rating may cause permanent damage to the device. Functional operation of the device should follow the conditions indicated in the "Recommended Operating Conditions", prolonged exposure to the absolute maximum rating may affect the reliability of the device.

Table 5: Absolute maximum ratings

Description	Comments	Min.	Max.	Unit
Supply voltage (VDDIO1, VDDIO2)		-0.3	3.9	V
Supply voltage (VBAT)		-0.3	3.9	V
Digital GPIO input	All digital GPIO pins	-0.3	VDDIO+0.3(*1)	V

Description	Comments	Min.	Max.	Unit
Analog HV (high voltage) input	CHIP_EN	-0.3	VBAT	V
TRX supply voltage	VDD_RF_2G4, VDD_VCO_2G4, VDD_PLL, VDD_AMS	-0.3	2	V
Analog LV (low voltage) input	XO_N, XO_P, RTC_XO_N, RTC_XO_P, ADC_IN, GPIO_2_X(*2)	-0.3	2	V
Input RF level	RF_TRX_2G4		5	dBm
ESD Human Body Model	All pins	-4000	4000	V
Storage temperature		-65	150	℃

*1: The corresponding VDDIO for a GPIO pin.

*2: When a mixed signal GPIO_2_X pin is used an analog input pin, the input voltage on that pin should less than 2V.

4.2 Recommended operating conditions

Table 6: Recommended operating conditions

Description	Min.	Typ.	Max.	Unit
VDDIO1, VDDIO2 (I/O supplies)	1.65	3	3.6	V
VBAT (The chip power supply)	1.65	3	3.6	V
Operating temperature	-40		85	°C

4.3 GPIO PAD characteristics

Measured at the following condition: Ta = 25°C, VDDIO1=VDDIO2 = VDDIO=3.0V, unless otherwise noted.

Table 7: GPIO PAD characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VIL	Input low voltage			0.3*VDDIO	V
VIH	Input High voltage	0.7*VDDIO			V
VOL	Output low voltage			0.4	V
VOH	output high voltage	VDDIO-0.4V			V
IOS (standard drive)	Output current @standard drive		2		mA
IOH (high drive)	Output current @high drive		4		mA
tLH/tHL (standard drive)	Rising time/Falling time @standard drive with 12pf load 10%~90%			4	ns
tLH/tHL (high drive)	Rising time/Falling time @high drive with 12pf load 10%~90%			2	ns
RPU	Pull-up resistance(*1) (VDDIO=3.3V)		20K		Ohm
RPD	Pull-down resistance(*2) (VDDIO=3.3V)		24K		Ohm
RPU	Pull-up resistance(*1) (VDDIO=3.0V)		22K		Ohm
RPD	Pull-down resistance(*2) (VDDIO=3.0V)		26K		Ohm
RPU	Pull-up resistance(1*) (VDDIO=1.8V)		44K		Ohm

Parameter	Description	Min.	Typ.	Max.	Unit
RPD	Pull-down resistance ** (VDDIO=1.8V)		56K		Ohm

*1: Characterized by measuring the pull-up current when the GPIO is connected to GND.

*2: Characterized by measuring the pull-down current when the GPIO is connected to VDDIO.

4.4 Buck converter characteristics

Measured at the following condition: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, L=4.7uH, C=4.7uF, unless otherwise noted.

Table 8: Buck converter characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Output current capability		0	15	30	mA
External capacitor range		1	4.7	20	uF
External inductor range		2	4.7	10	uH
Inductor ESR			300	650	MOhm
Inductor saturation current		150		500	mA
VBAT		1.65	3.0	3.6	V
Output voltage range		1	1.2	1.4	V
Efficiency @3.0V VBAT			83		%
Efficiency @1.8V VBAT			89		%
Startup time			250	400	us
Overshoot at startup			0		V

4.5 11-bit SAR ADC characteristics

Measured at the following condition: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, VREF=on-chip V1P0, unless otherwise noted (If the ADC is used, VBAT should not be larger than 3.0V).

Table 9: ADC characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Physical bits			11		bits
ENOB	64 KSPS		9.7(*1)		bits
	32 KSPS		10.3(*1)		bits
SINAD	64 KSPS		60(*1)		dB
	32 KSPS		63(*1)		dB

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Current from VBAT	64 KSPS		123(*1)		uA
	32 KSPS		122(*1)		uA
Current from 1.2V VDD	64 KSPS		900(*1)		nA
	32 KSPS		460(*1)		nA
Conversion latency		13			clock cycles
Conversion rate			64		KSPS
INL		-2		2	LSB
DNL		-1		1	LSB
VREF			1.0		V
Input voltage range		0		2*VREF	V
Input channels				12 (*2)	-
Input signaling	single-ended			2	V
Input offset			10		mV

*1: Based on simulation.
*2: The number of channels depends on the package.

4.6 VBAT monitoring characteristics

Measured at: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, unless otherwise noted.

Table 10: VBAT monitoring characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V1P0 as the reference		2.3		mV/LSB
Range	Input to ADC = 0.4*VBAT. The input range of ADC is 0V - 2V (FS).	1.7		3.6	V
Accuracy	With VREF calibration only	-3.3	1.1	3.3	%
	With ADC offset and VREF calibration	-0.6	0.2	0.6	%

4.7 Device temperature monitoring characteristics

Measured at: Ta = 25°C, VBAT=VDDIO=3.0V, unless otherwise noted.

Table 11: Temperature monitoring characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V1P0 as the reference		-0.25		°C /LSB
Range		-40		85	°C
Accuracy	With VREF calibration only	-3	1	3	%
	With ADC offset and VREF calibration	-1.8	0.6	1.8	%

4.8 32kHz RC oscillator characteristics

Measured at the following condition: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, unless otherwise noted.

Table 12: 32kHz RC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Oscillation frequency(*1)	After one-time tune	27	32	39	kHz
Temperature coefficient			-1168.8	-1829	ppm/°C

*1: The Min and Max are over a temperature range of [-40°C -85°].

4.9 32MHz crystal oscillator characteristics

Measured at the following condition: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, unless otherwise noted.

Table 13: 32MHz Crystal oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency			32		MHz
Crystal frequency tolerance		-40		40	ppm
ESR			60		Ohm
Lm, motional inductance			17	35	mH
Cm, motional capacitance			2.2	3	fF
Cl crystal load capacitance	differential			8	pF
C0			0.7	3	pF

Parameter	Test conditions	Min.	Typ.	Max.	Unit
On-chip CI	differential, programmable in 0.5pF steps	0.5		8	pF
Start-up time			500	1000	us

Note: Crystal datasheet must meet specified requirements for frequency, frequency tolerance, ESR, Lm, Cm, CI, and C0.

4.10 32MHz RC oscillator characteristics

Measured at the following condition: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, unless otherwise noted.

Table 14: 32MHz RC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	Programmable with 1MHz resolution	16	32	48	MHz
Temperature coefficient			-0.1344		%/°C

4.11 32.768kHz RTC oscillator characteristics

Measured at the following condition: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, unless otherwise noted.

Table 15: 32.768kHz RTC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency			32.768		kHz
Crystal frequency tolerance	Including aging and temp. drift	-500		500	ppm
ESR			30	100	kOhm
On-chip CI	differential, programmable in 0.5pF steps	0.5		16	pF
CI crystal load capacitance	differential	4	7	12	pF

Note: Crystal datasheet must meet specified requirements for frequency, frequency tolerance, ESR, and CI.

4.12 RF performance characteristics

Characteristics are measured over recommended operating conditions unless otherwise specified. The typical value is referred to at TA = 25°C and VBAT = 3.0V. The specifications are valid for -45°C ⩽ TA ⩽ +85°C and 1.8V ⩽ VBAT ⩽ 3.6V. All performance data are measured via an evaluation board with a 50-Ohm antenna connector.

4.12.1 General RF characteristics

Table 16: General RF characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Radio-frequency range		2320		2650	MHz
RF PLL channel spacing	channel spacing is user programmable		1		MHz
Frequency modulation deviation	1Mbps PHY		±250		kHz
Frequency modulation deviation	2Mbps PHY		±500		kHz
Data Rate		125		2000	kbps
RSSI dynamic range		-100		-25	dB
RSSI accuracy			2		dB
RSSI resolution			1		dB

4.12.2 RF Receiver Performance Characteristics

Measured at: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, fRF=2440MHz, unless otherwise noted.

Table 17: RF receiver performance characteristics

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
Maximum receive signal level	1Mbps			5		dBm
Sensitivity - typ. current setting	2Mbps	Average of all channels. Using on-chip DCDC. Measured at SMA connector, BER=1e-3. Typical current settings.		-94.5 (*1)		dBm
	1Mbps			-97.5 (*1)		dBm
	500kbps			-100		dBm
	125kbps			-104		dBm
Sensitivity Improvement delta - max. current setting		Set LNA bias current to maximum		-0.5		dB

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
Sensitivity build-to-build variation		Chip variation + matching component variation	-0.5		0.5	dB
I/D Co-channel	2Mbps	Desired signal at -67dBm, modulated interferer in channel, BER=1e-3		-7.6		dB
I/D Selectivity, +/- 2MHz				8 / 4		dB
I/D Selectivity, +/- 4MHz				45 / 15		dB
I/D Selectivity, +/- 6MHz				49 / 35		dB
I/D Selectivity, +/- 8MHz				52 / 43		dB
I/D Selectivity, +/- 16MHz				44 / 36		dB
I/D Selectivity, +/- 32MHz				53 / 51		dB
I/D Selectivity, +/- (10...20) MHz				41		dB
I/D Selectivity, +/- (21+) MHz				50		dB
I/D Selectivity, image frequency				15		dB
I/D Selectivity, adjacent (2MHz) to image frequency				35		dB
I/D Co-channel	1Mbps	Desired signal at -67dBm, modulated interferer in channel, BER=1e-3		-6.2		dB
I/D Selectivity, +/- 1MHz				5.6 / 3.6		dB
I/D Selectivity, +/- 2MHz				42 / 23		dB
I/D Selectivity, +/- 3MHz				47 / 32		dB
I/D Selectivity, +/- 4MHz				50 / 37		dB
I/D Selectivity, +/- 16MHz				54 / 53		dB
I/D Selectivity, +/- (5...10) MHz				45		dB
I/D Selectivity, +/- (11...20) MHz				55		dB
I/D Selectivity, +/- (21+) MHz				56		dB
I/D Selectivity, image frequency				23		dB

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
I/D Selectivity, adjacent (1MHz) to image frequency				32		dB
I/D Co-channel	500kbps	Desired signal at -72dBm, modulated interferer in channel, BER=1e-3		-2.5		dB
I/D Selectivity, +/- 1MHz				9 / 7		dB
I/D Selectivity, +/- 2MHz				47 / 32		dB
I/D Selectivity, +/- 3MHz				51 / 39		dB
I/D Selectivity, +/- 4MHz				54 / 43		dB
I/D Selectivity, +/- 16MHz				49 / 44		dB
I/D Selectivity, +/- 32MHz				61 / 60		dB
I/D Selectivity, +/- (5...10) MHz				48		dB
I/D Selectivity, +/- (11...20) MHz				52		dB
I/D Selectivity, +/- (21+) MHz				55		dB
I/D Selectivity, image frequency				32		dB
I/D Selectivity, adjacent (1MHz) to image frequency				39		dB
I/D Co-channel	125kbps	Desired signal at -79dBm, modulated interferer in channel, BER=1e-3		-1.5		dB
I/D Selectivity, +/- 1MHz				12.5/ 10.5		dB
I/D Selectivity, +/- 2MHz				51 / 33		dB
I/D Selectivity, +/- 3MHz				54 / 39		dB
I/D Selectivity, +/- 4MHz				57 / 46		dB
I/D Selectivity, +/- 16MHz				49 / 45		dB
I/D Selectivity, +/- 32MHz				63 / 62		dB
I/D Selectivity, +/- (5...10) MHz				52		dB
I/D Selectivity, +/- (11...20) MHz				55		dB

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
I/D Selectivity, +/-(21+) MHz				68		dB
I/D Selectivity, image frequency				39		dB
I/D Selectivity, adjacent (1MHz) to image frequency				46		dB
Intermodulation	2Mbps	Desired at 2402MHz, -64dBm. Two interferers at 2408MHz (N+3) and 2414MHz (N+6) at the given power level		-32		dBm
	1Mbps	Desired at 2402MHz, -64dBm. Two interferers at 2405MHz (N+3) and 2408MHz (N+6) at the given power level		-27		dBm
Out-of-band blocking	1Mbps	30MHz to 2000MHz, step = 10MHz		-10		dBm
		2003MHz to 2399MHz, step = 3MHz		-5		dBm
		2484MHz to 2997MHz, step = 3MHz		-10		dBm
		3000MHz to 12.75GHz *(2), step = 25MHz		-8		dBm

*1: LNA max gain setting

4.12.3 RF Transmitter Performance Characteristics

Measured at: Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, fRF=2440MHz, unless otherwise noted.

Table 18: RF transmitter performance characteristics

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
Maximum output power		Averaged over the band and build		3		dBm
Minimum output power				-35		dBm
Output power variation over the band		2402MHz - 2480MHz	-0.5		0.5	dB
Output power build-to-build variation		Chip variation + matching	-0.5		0.5	dB

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
		component variation				
In-band spurious emission	2Mbps, @ Pout, max	N +/- 4MHz		-44		dBm
		N +/- 5MHz		-46		dBm
		N +/- ≥6MHz		-48		dBm
In-band spurious emission	1Mbps, @ Pout, max	N +/- 2MHz		-38		dBm
		N +/- ≥3MHz		-41		dBm
Out-of-band spurious emission	@ Pout, max	f<1GHz, outside restricted bands		-67		dBm
		f<1GHz, restricted bands ETSI		-77		dBm
		f<1GHz, restricted bands FCC		-63		dBm
		f>1GHz, including harmonics		-44		dBm
		HD2		-48		dBm
		HD3		-45		dBm

4.13 System power consumption

Currents are measured at Ta = 25°C, VBAT=3.0V, VDDIO1=VDDIO2=VDDIO=3.0V, CPU subsystem clocked at 32MHz and peripherals at 16MHz, with internal DC-DC converter enabled unless otherwise noted.

Table 19: System power consumption

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
I_VBAT	Current consumption	Chip disabled, CHIP_EN=0V		20		nA
		Deep-sleep with 32kHz RC, sleep timer (*1)		0.52 (*2)		uA
		Deep-sleep with 32.768kHz RTC, sleep timer (*1)		0.64 (*2)		uA
		Deep-sleep with 32.768kHz RTC, sleep timer, 16kB retention (*1)		0.80 (*2)		uA
		Deep-sleep with 32.768kHz RTC, sleep timer, 32kB retention (*1)		0.94 (*2)		uA
		Deep-sleep with 32.768kHz RTC, sleep		1.34 (*2)		uA

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
		timer, 32kB retention, BOD enabled (*1)				
		Idle. DCDC powers up the core and RAM, XO 32MHz not running		500 (*2)		uA
		Idle. CPU at 32MHz and peripheral at 16MHz, XO32 MHz running		1.1		mA
		Active. CPU at 32MHz running from RAM and peripheral at 16MHz, XO32 MHz running		2.5		mA
		CPU power consumption		45		uA/MHz
		2.4GHz RX mode - 1Mbps (*3)		5(*5)/6.4(*6)		mA
		2.4GHz RX mode - 1Mbps (*4)		5.3(*5)/6.7(*6)		mA
		2.4GHz RX mode - 2Mbps		6.1(*5)/7.5(*6)		mA
		2.4GHz TX mode - 1Mbps, Pout=0dBm		4.9(*5)/6.3(*6)		mA
		2.4GHz TX mode - 2Mbps, Pout=0dBm		4.9(*5)/6.3(*6)		mA
I_VDDIO(*7)	VDDIO current consumption	Chip disabled, CHIP_EN=0V		10		nA

Note:

*1: VDD_AONPD is in dynamic mode.
*2: Number is based on C/S measurement.
*3: Settings for -97dBm sensitivity.
*4: Settings for -97.5dBm sensitivity.
*5: CPU at idle (WFI).
*6: CPI active running.
*7: Sum of the currents of VDDIO1 and VDDIO2.

4.14 ESD characteristics (all pins)

- HBM (human body model): Sensitivity pass +/-4000V, Class-3A (Reference ESDA/JEDEC JS-001-2017)
- CDM (charge device model): Sensitivity Pass: ±1000V, Class-C3 ESDA/JEDEC JS-002-2018

5 Ordering Information

Table 20 contains information on the device order part number and the feature difference. Figure 23 shows the decoding of the part number. The package information can be found in Table 21.

Table 20: Device order part number and feature difference

Part number	Bluetooth 5 (Y/N)	Long range*	SDR (Y/N)	Secure boot and ISP	ROM mask version
IN612L-Q1-R-G4C0I	Yes	Yes	Yes	Yes	C0
IN610L-Q1-R-G4C0I	Yes	Yes	No	Yes	C0
IN610-Q1-R-G4C0I	Yes	No	No	Yes	C0

* Long-range modes (125Kbps and 500Kbps)

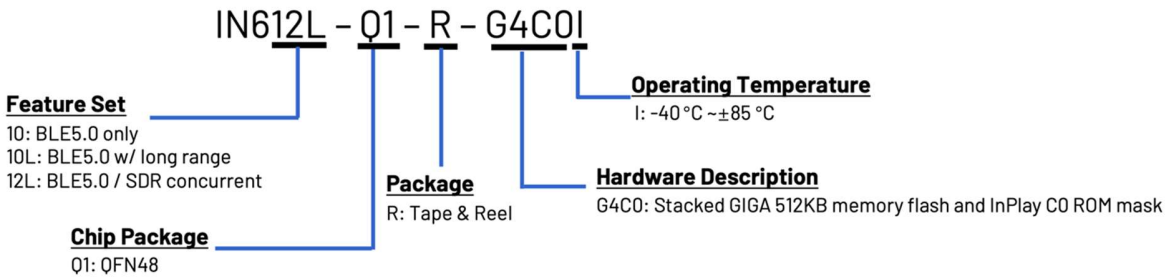
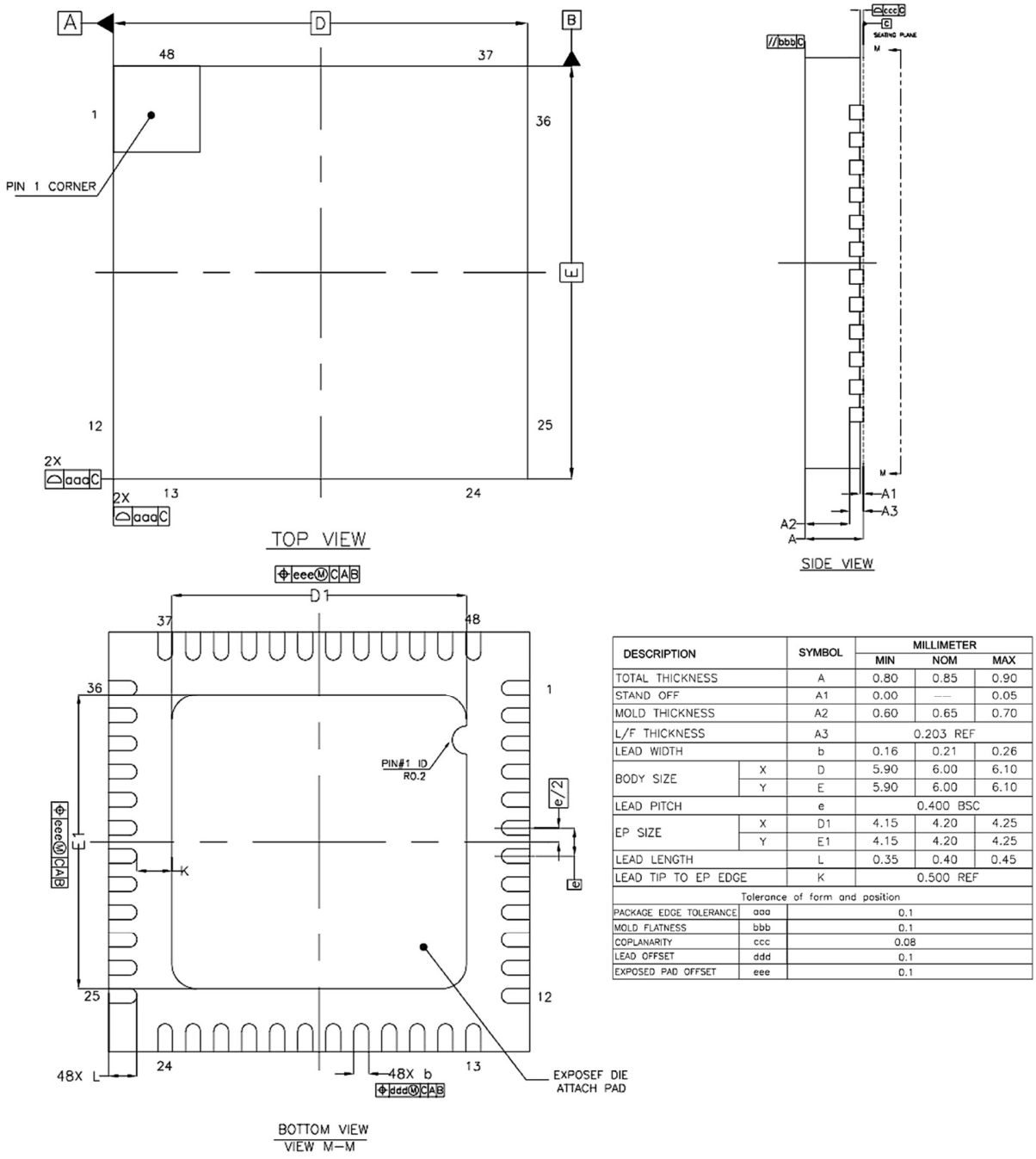


Figure 23: Decoding of the device order part number

6 Packaging

The device will be offered in QFN48 packages. The QFN package is RoHS/green compliant.

6.1 Package drawing – QFN48



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	—	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.16	0.21	0.26
BODY SIZE	X	D	5.90	6.00	6.10
	Y	E	5.90	6.00	6.10
LEAD PITCH		e	0.400 BSC		
EP SIZE	X	D1	4.15	4.20	4.25
	Y	E1	4.15	4.20	4.25
LEAD LENGTH		L	0.35	0.40	0.45
LEAD TIP TO EP EDGE		K	0.500 REF		
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa		0.1		
MOLD FLATNESS	bbb		0.1		
COPLANARITY	ccc		0.08		
LEAD OFFSET	ddd		0.1		
EXPOSED PAD OFFSET	eee		0.1		

Figure 24: IN610 IN610L IN612L QFN48 6mmx6mm package outline drawing

Table 21: IN610/IN610L/IN612L 6x6 QFN48 package information

Parameter	Value	Units	Tolerance
Package Size	6.00 x 6.00	mm	±0.10
QFN Pad Count	49		
Total Thickness	0.85	mm	±0.05
QFN Pad Pitch	0.4	mm	
Lead Width	0.21	mm	±0.05
Exposed Pad Size	4.20 x 4.20	mm	±0.05

6.2 IC marking

The IN610/IN610L/IN612L devices are marked as described below, as shown in Figure 25.

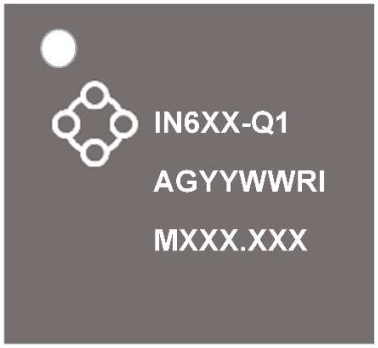


Figure 25: IN610/IN610L/IN612L package marking

Table 22: IN610/IN610L/IN612L marking description

Abbreviation	Definition and implemented codes
IN6XX-Q1	InPlay SwiftRadio™ SoC product name
AG	Stack flash vendor code
YY	Year code
WW	Week code
R	Die version
I	Temperature code
MXXX.XXX	Production control code

6.3 Box package dimension

Defined here are the device package size for the reel, inner box, and outer box.

Table 23: IN610/IN610L/IN612L package size for the reel, inner box, and outer box

Package	Reel size	Reel size	Inner box size	Outer box size
QFN	13”	4000	4000	40000

7 Reference Design

7.1 IN610/IN610L/IN612LQFN48 reference schematic

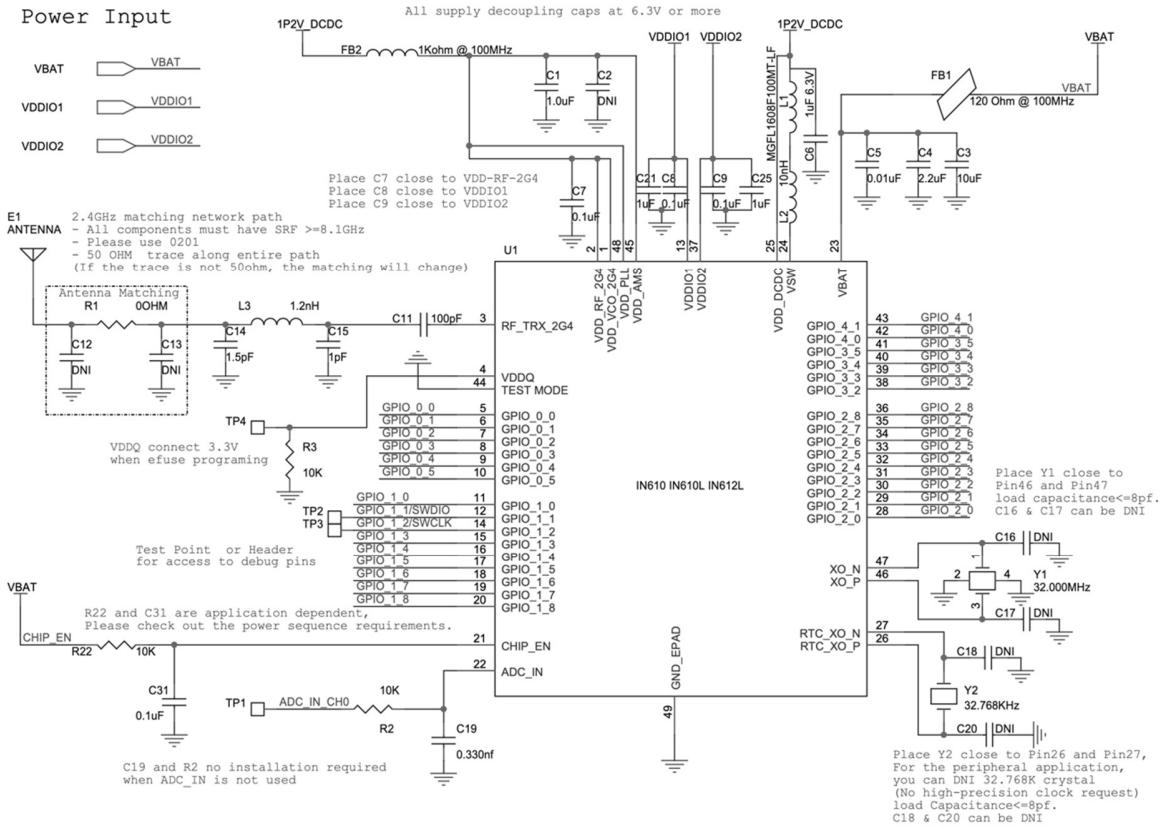


Figure 26: IN610/IN610L/IN612L QFN48 reference schematic

Table 24: IN610/IN610L/IN612L reference design BOM of QFN48

Reference	Value	Description	Vendor	Part number	Footprint
C1, C6, C21, C25	1uF	Cap CER 1uF 25V X5R 0402	TDK	C1005X5R1E105KT000E	C0402
C2, C12, C13, C10, C16, C17, C18, C20	DNI	Do not insert			

Reference	Value	Description	Vendor	Part number	Footprint
C3	10uF	Cap CER 10uF 6.3V JB	TDK	C1608JB0J106M080AB	C0603
C4	2.2uF	Cap CER 2.2uF 6.3V X7S	TDK	C1005X7S0J225K050BC	C0402
C5	0.01uF	Cap CER 10000pF 10V X7R	Murata	GCM033R71A103KA03D	C0201
C7, C8, C9, C31	0.1uF	Cap CER 0.1uF 6.3V X6S	Murata	GRM033C80J104ME15D	C0201
C15	1.0pF	Cap CER 1pF 25V C0G/NP0	Murata	GJM0335C1E1R0BB0	C0201
C11	100PF	Cap CER 100PF 50V C0G/NP0	Murata	GRM0335C1H101JA01D	C0201
C14	1.5pF	Cap CER 1.5PF 50V C0G/NP0	Murata	GRM0335C1H1R5BA01D	C0201
C19	0.330nF	Cap CER 330PF 25V X7R	TDK	C0603X7R1E331M030BA	C0201
E1		Antenna 2.4~2.5GHz 50Ohm			
FB1	120 Ohms @ 100 MHz	120 Ohms @ 100 MHz 1 Ferrite Bead	Murata	BLM15AG121SN1D	L0402
L1	10uH	Fixed 10uH 400mA 550MOhm	Microgate	MGFL1608F100MT-LF	L0603
L2	10nH	Fixed 10NH 500mA 350 MOhm	Murata	LQG15HN10NJ02D	L0402
L3	1.2nH	Fixed IND 1.2nH 600mA 150MOhm SM	Murata	LQP03TG1N2B02D	L0201
FB2	1kOhm@ 100MHz	Ferrite bead 1 kOhm	Murata	BLM15AG102SH1D	L0402
R1	0Ohm	RES 0 Ohm jumper 1/20W	Bourns	CR0201-J/-000GLF	R0201
R2, R3, R22	10K	Res SMD 10K Ohm 5% 1/10W	Panasonic	ERJ-2GEJ103X	R0402
TP1, TP2, TP3, TP4		Test Point			
U1	IN61XX	BLE Chip QFN6x6 48pins	InPlay	The IN610, IN610L and IN612L (IN6XX devices) share the same hardware (die) version.	QFN48

Reference	Value	Description	Vendor	Part number	Footprint
Y1	32 MHz	crystal 32 MHz 6pF SMD	NDK	NX1612SA-32.000MHZ-CHP-CIS-3	4-SMD
Y2	32.768 kHz	crystal 32.7680kHz 7pF SMD	ECS	ECS-327-7-34B-C-TR	2-SMD

8 Layout

To ensure device performance, it is recommended to follow the general printed circuit board layout guidelines.

8.1 Layer stack-up

The recommendations in this document refer to the four-layer IN610 IN610L IN612L PCB based on standard flame retardant 4 (FR4) materials, a technology commonly used in commercial applications.

Table 25: PCB layer stack-up

PCB Layer stack-up					
Layer	Purpose	Material	Thickness	Thickness control	Adjust to get desired total PCB thickness
Top layer +Plating	Signal	1/2 oz Cu	1.4	Yes	No
Dielectric		Roger 4003C	8	Yes	No
Internal Layer 1	GND	1/2 oz Cu	0.7	No	Yes
Dielectric		RF4	42	No	Yes
Internal Layer 1	Signal/power	1/2 oz Cu	0.7	No	Yes
Dielectric		RF4	8	No	Yes
Bottom Layer + Plating	Signal/power	1/2 oz Cu	1.4	No	Yes
		Total thickness	62		

8.2 Crystal

There is a high-speed 32MHz crystal in the system, the parasitic nature of the clock trace affects the oscillation, and the crystal should be placed as close as possible to the chip. Too-wide traces can cause excessive capacitance, while too-narrow traces can cause parasitic inductance of the clock traces. For short clock traces, use a trace width of approximately 10 mils (0.010 inches or 0.254 mm). Keep the crystal tuning capacitor close to the crystal pad.

Avoid passing through the crystal lines on adjacent layers. Keep the ground plane below the crystalline to improve the return path.

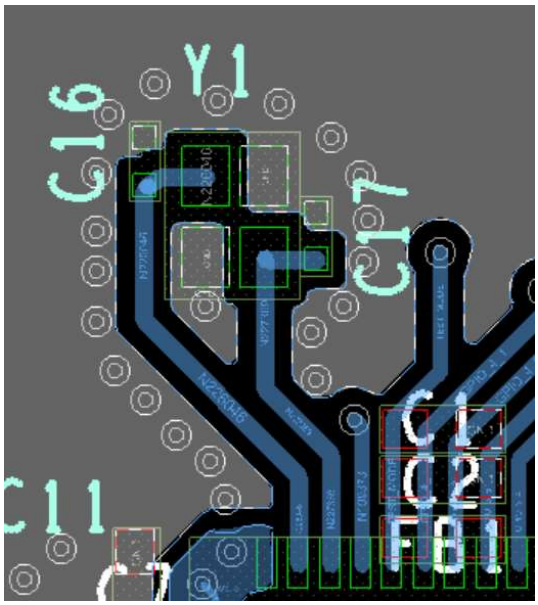


Figure 27: 32MHz crystal

The slow clock signal line must be as short as possible. The trace of the slow clock signal should have a ground plane on each side of the signal trace to reduce unwanted signal coupling. To reduce the capacitive coupling of unwanted signals to the clock line, the slow clock traces must not be higher or lower than other signals (especially digital signals).

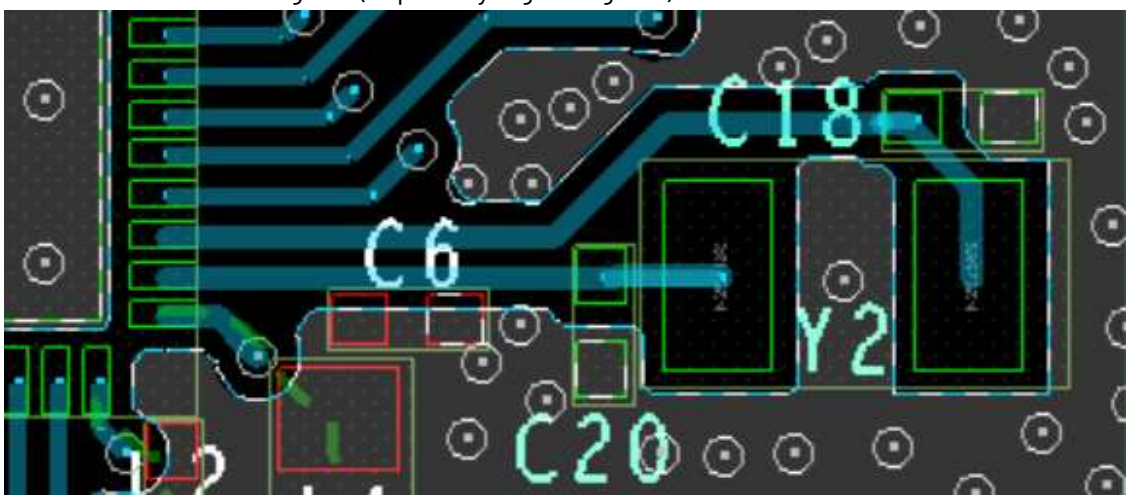


Figure 28: 32.768kHz crystal

8.3 RF trace

Place the RF path on the top layer (component side) and keep the trace as short as possible. Referring to solid ground (Layer 2), the impedance of the RF trace must be controlled to 50 Ohms. In addition, ground Vias are required for better RF isolation.

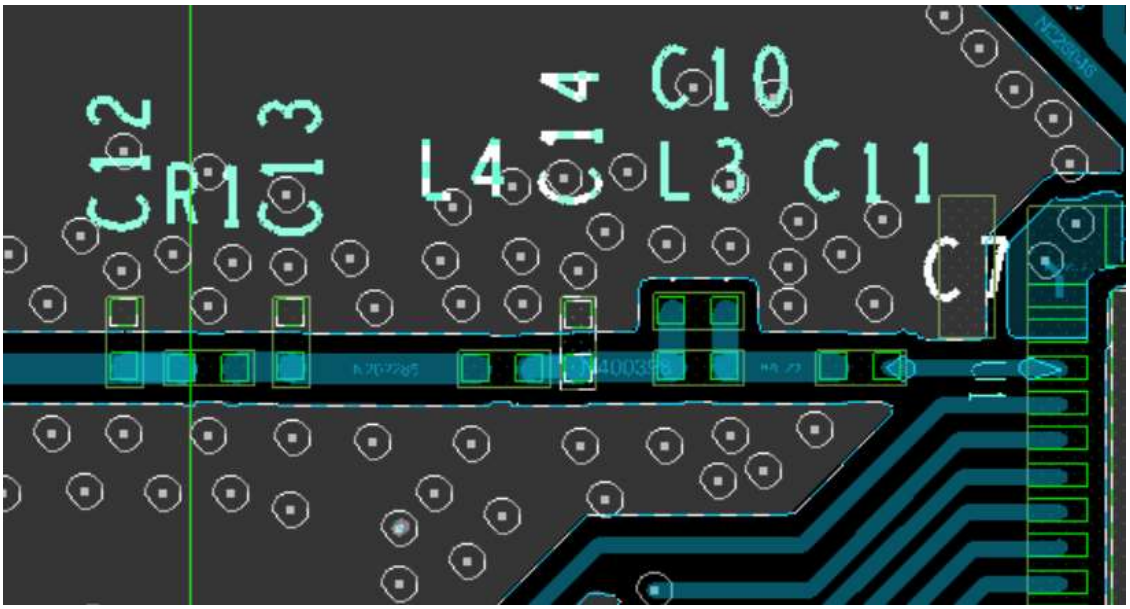


Figure 29: RF trace

8.4 Antenna

The antenna is a key component in wireless system design to make sure the device will perform as expected. Make sure to select the antenna that covers the appropriate frequency band from 2.350GHz to 2.550GHz. Talk to the antenna supplier and make sure he understands that the antenna must cover the entire frequency range. Also, make sure the antenna is designed for a 50Ω impedance system. Make sure the PCB pads to which the antenna is connected are properly designed to have a 50Ω impedance. The antenna supplier must specify the pad size, the pitch from the pad to the ground reference plane, and the spacing from the pad edge to the ground fill on the same layer as the pad. In addition, since the ground reference plane from the antenna pad to the 50Ω trace of the IN6I2NL may be on a different layer than the ground reference of the antenna pad, ensure that the pad design has an appropriate transition from pad to pad 50Ω trace. Make sure the antenna-matching components are placed as close as possible to the antenna pads. Always consult with an antenna expert on antenna matching to ensure the best RF performance.

8.5 PMU LDO output

Shorter trace lengths should be used to avoid overload. The 1.2V output needs to be fully filtered through a 4.7uf capacitor, then connect to the DCDC & RF power pins, The bigger inductor should use the low DRC winding inductor.

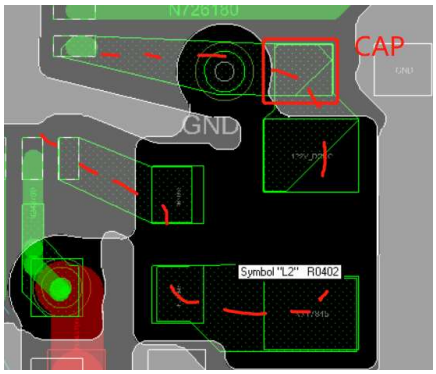


Figure 30: IP2V-DCDC output

Note that the PMU is a switching regulator that produces noise in the 2.4 GHz receive band. Therefore, RF routing, components, and antennas must be as far as possible from the PMU and its components (L1, L2, and C6).

8.6 VBAT power supply

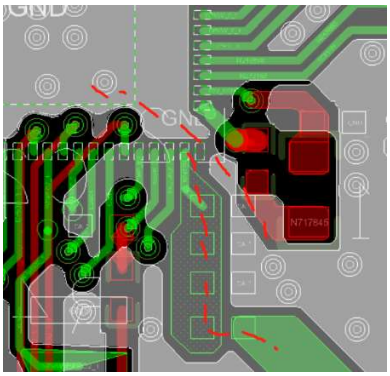


Figure 31: VBAT trace

The VBAT power supply is the same as LDO 1.2V output. This is the power supply for the PMU, and the noise of the PMU is fed back to the power supply pin. FB2 is used to suppress noise and prevent it from radiating from the power supply path. Therefore, the RF path should also be kept away from the VBAT supply path and FB2, C3, C4, and C16.

The filter capacitor on the VBAT pin needs to be as close as possible, and the ground pads of the capacitors need to be close to the chip ground. This is very important for the internal RC clock.

8.7 Power supply

Below routing requirements for power supplies shall apply to the IN610 IN610L IN612L device:

- Short power supply trace length

- Decoupling capacitor placed as close as possible to the device
  - C7 close to VDD_RF_2G4
  - C9 close to VDDIO2
  - C8 close to VDDIO1
  - C1 and C2 close to VDD_AMS

The most common ground loop problem occurs when the ground loop current has a longer return path due to placing the DC bypass capacitor to the ground.

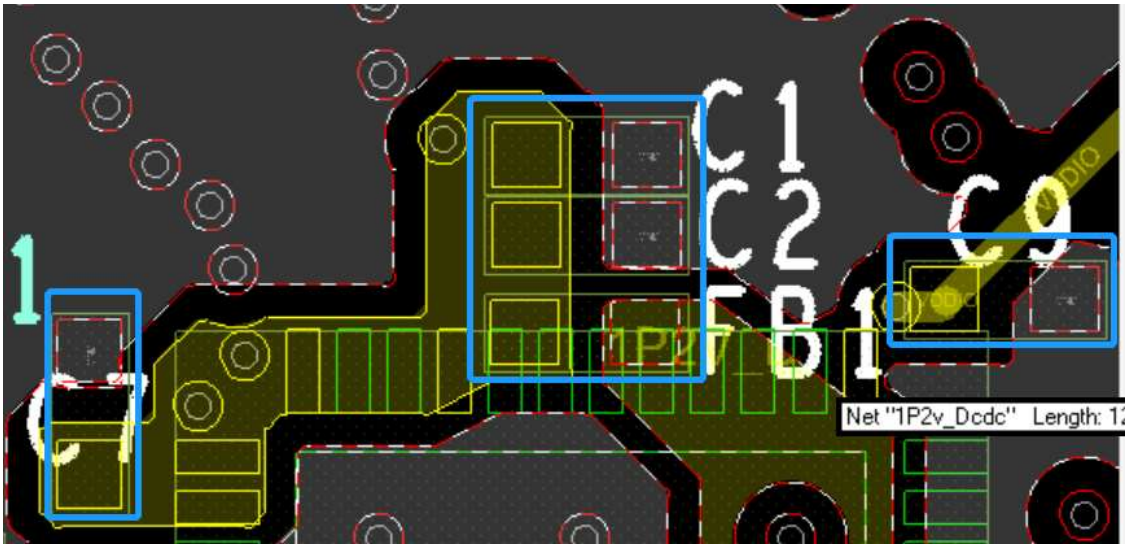


Figure 32: Placement with RF power routing

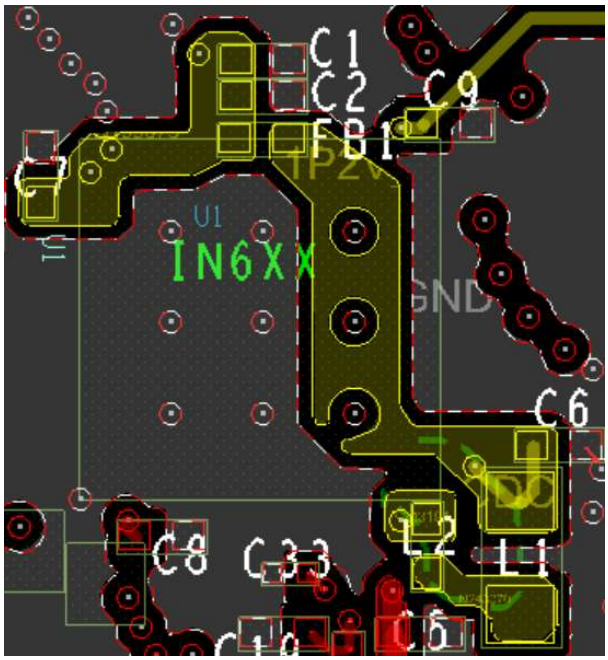


Figure 33: Routing of 1P2V supply

8.8 Thermal pad VIAs

To increase the ground coupling, add at least 9 Vias directly to the SoC's thermal pad to the solid ground, as shown in Figure 34.

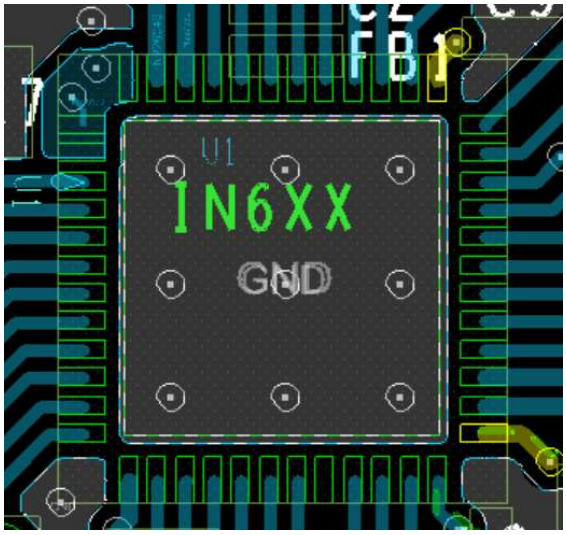


Figure 34: Thermal pad vias

8.9 Ground

Use a dedicated one layer for the ground plane. Make sure this ground plane is not broken down by the route. The power supply can be routed on all layers except the ground floor. The power path should be a heavy copper-filled plane to ensure the lowest possible inductance.

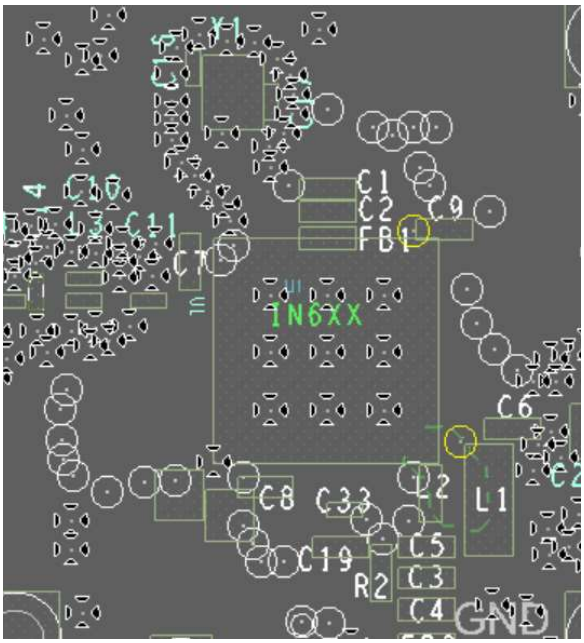


Figure 35: Example of the ground layer

9 Reflow Profile Information

This section provides guidelines for reflow processes in getting the InPlay Device soldered to the user's design.

9.1 Storage condition

9.1.1 Moisture barrier bag before opened

A moisture barrier bag must be stored at a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

9.1.2 Moisture barrier bag open

Humidity indicator cards must be blue, < 30%.

9.2 Stencil design

The recommended stencil is laser-cut, stainless-steel type with a thickness of 100μm to 130μm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with a bottom opening 25μm larger than the top can be utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

9.3 Baking conditions

This module is rated at MSL level 3. After the sealed bag is opened, no baking is required within 168 hours so long as the devices are held at <= 30°C /60% RH or stored at <10% RH.

The module will require baking before mounting if:

The sealed bag has been open for > 168 hours.

Humidity Indicator Card reads >10%.

SIPs need to be baked for 8 hours at 125°C.

9.4 Soldering and reflow conditions

9.4.1 Reflow oven

It is strongly recommended that a reflow oven equipped with more heating zones and a Nitrogen atmosphere be used for lead-free assembly. Nitrogen atmosphere has been shown to improve wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items should also be observed in the reflow process:

1. Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V type 3, no clean paste.
2. Allowable reflow soldering times: Three times based on the following reflow soldering profile (as shown in Figure 36).
3. Temperature profile: Reflow soldering shall be done according to the following temperature profile (as shown in Figure 36).
4. Peak temperature: 250°C.

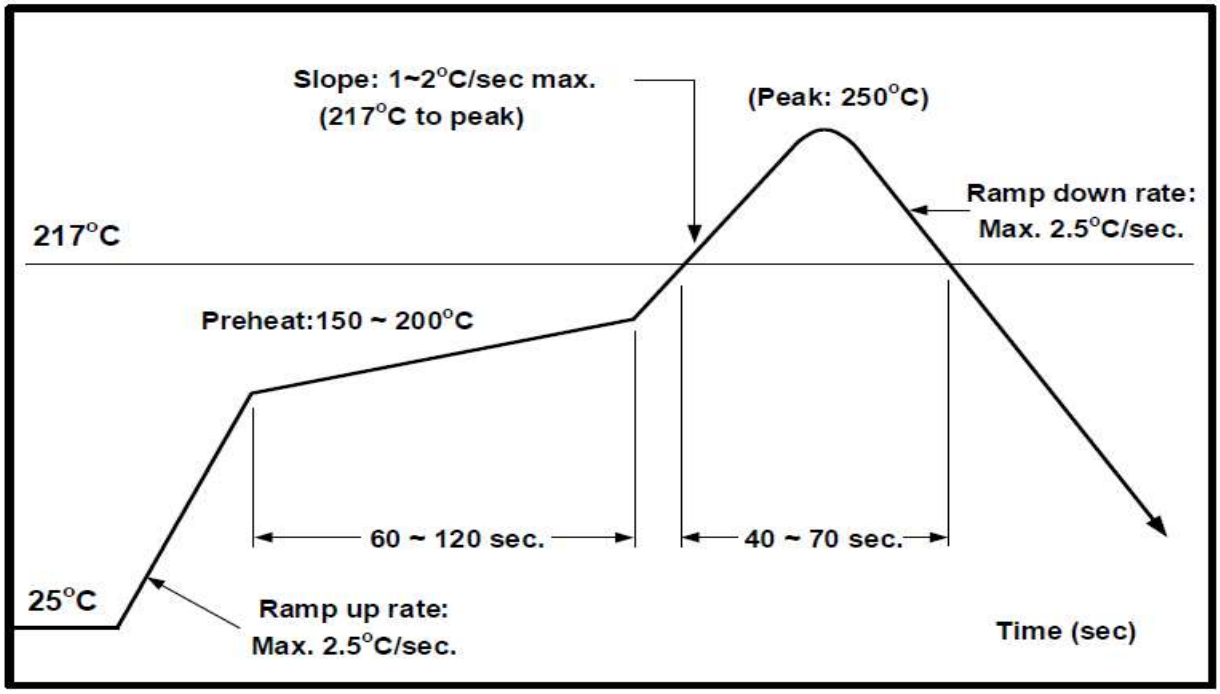


Figure 36: Solder reflow profile

10 Revision History

Revision	Description	Date	Drafted by
V1.0	Initial Version	6/30/2020	
V1.10	Modify the document format	03/21/2022	
V1.20	Functional descriptions were enhanced for better user understanding.	03/24/2023	
V1.30	Update power sequence description Update GPIO pad characteristics for Pull-up & Pull-down resistance Add JTAT trace in pinmux Update 32KHz RC characteristics Add active power consumption	05/21/2023	
V2.0	Major updates	06/29/2023	

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